Advanced Computer Architecture (0630561)

Lecture 15

Interconnection Networks

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Interconnection Networks:

Multiprocessors INs can be classified based on:

1. Mode of Operation:

– **Synchronous**: a single global clock is used by all components in the system.

– **Asynchronous**: No global clock required. Hand shaking signals are used to coordinate the operation of asynchronous systems.

2. Control Strategy:

– **Centralized**: one central control unit is used to control the operations of the components of the system.

– **Decentralized**: the control function is distributed among different components in the system.

Interconnection Networks:

3. Switching Techniques:

– **Circuit switching**: a complete path has to be established prior to the start of communication between a source and a destination.

– **Packet switching**: communication between a source and a destination takes place via messages divided into smaller entities, called packets.

4. Topology:

– Describes how to connect processors and memories to other processors and memories. INs can be classified as;

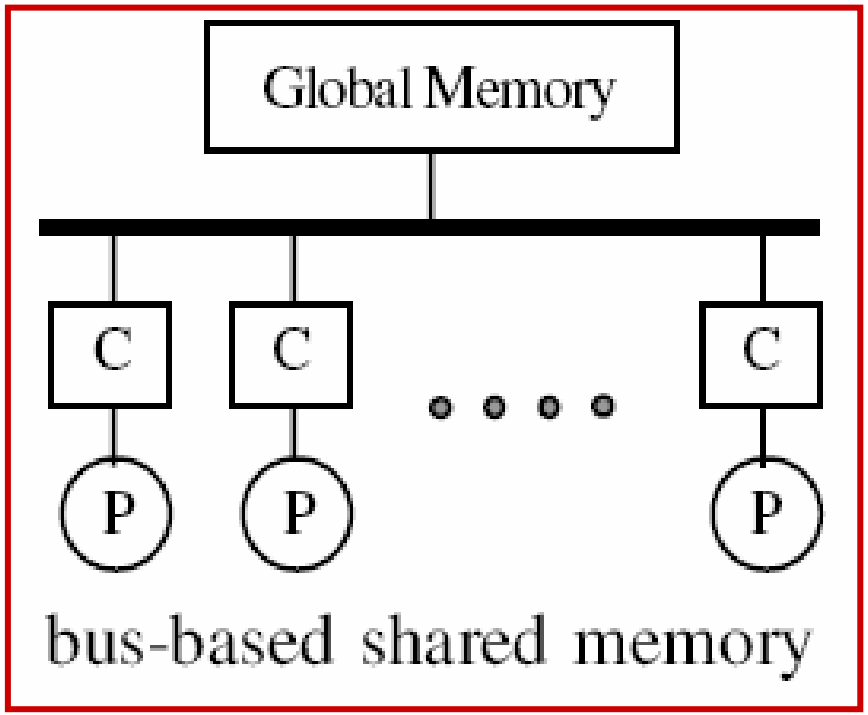
– **Static**: direct fixed links are established among nodes to form a fixed network.

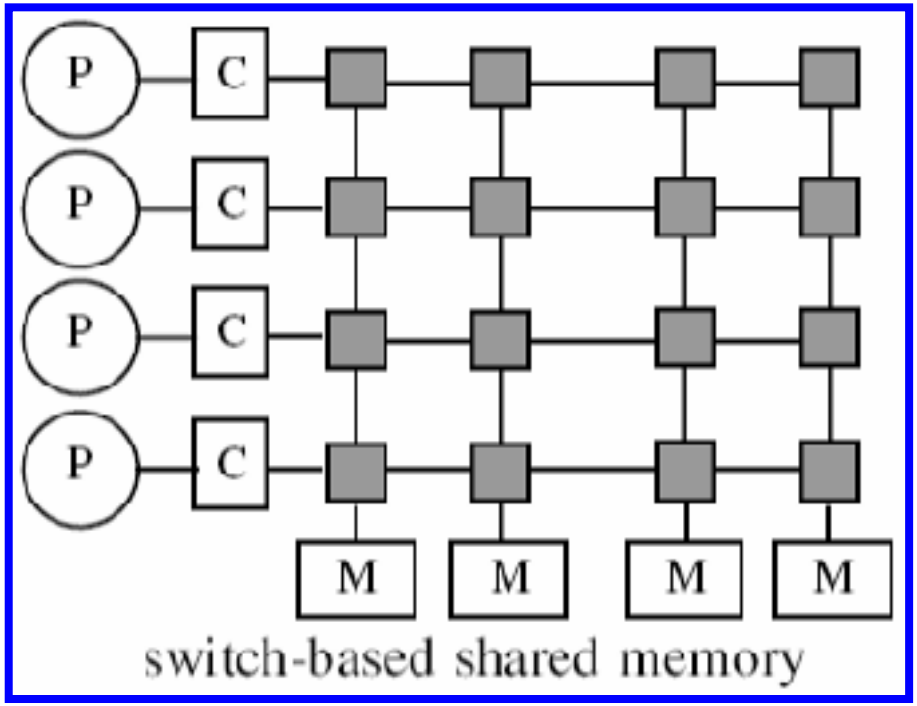
– **Dynamic**: connections are established when needed.

Shared memory systems can be designed using bus-based or switch-based INs.

The simplest IN for shared memory systems is the bus. However, the bus may get saturated if multiple processors are trying to access the shared memory (via the bus) simultaneously.

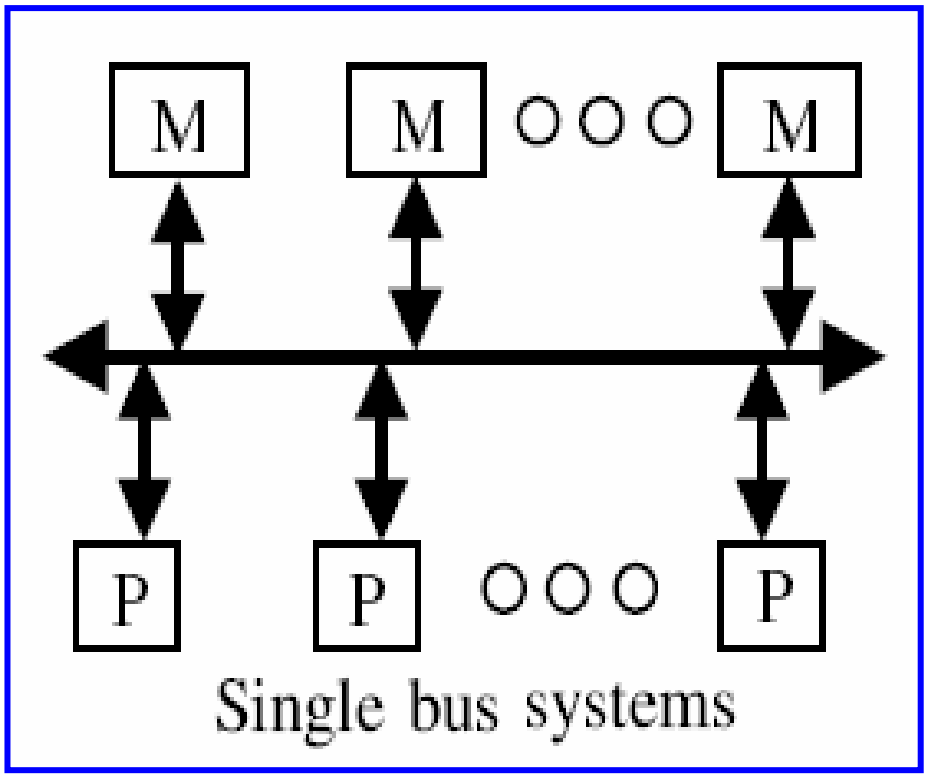
A crossbar switch can be visualized as a mesh of wires with switches at the points of intersection.

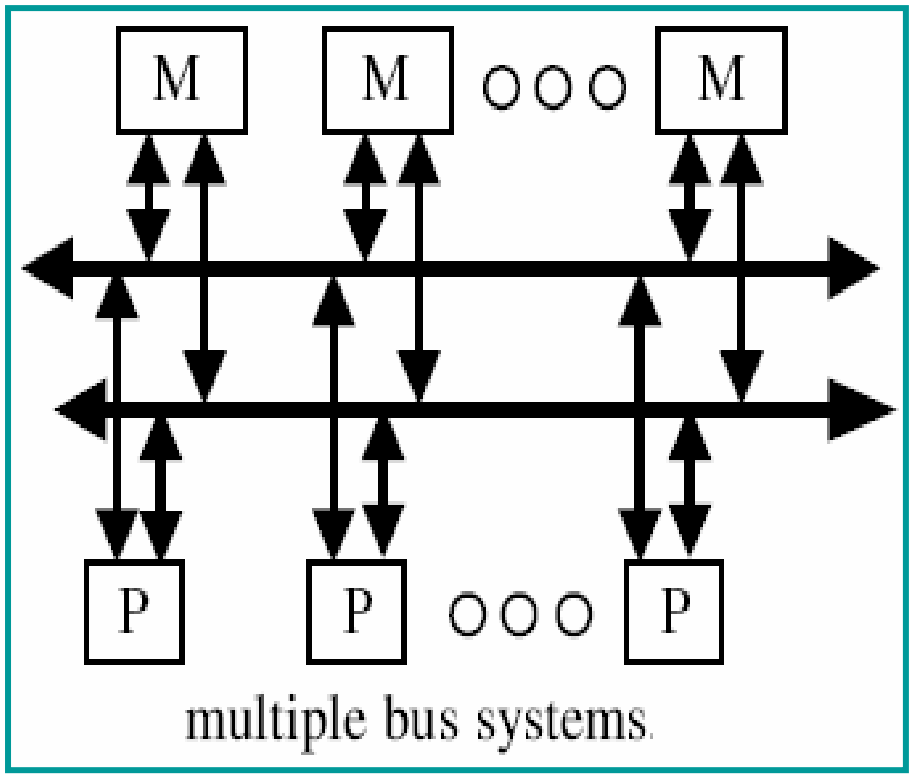




Single-bus & Multi-bus Systems:

This figure shows bus-based systems when a single bus is used versus the case when multiple buses are used.



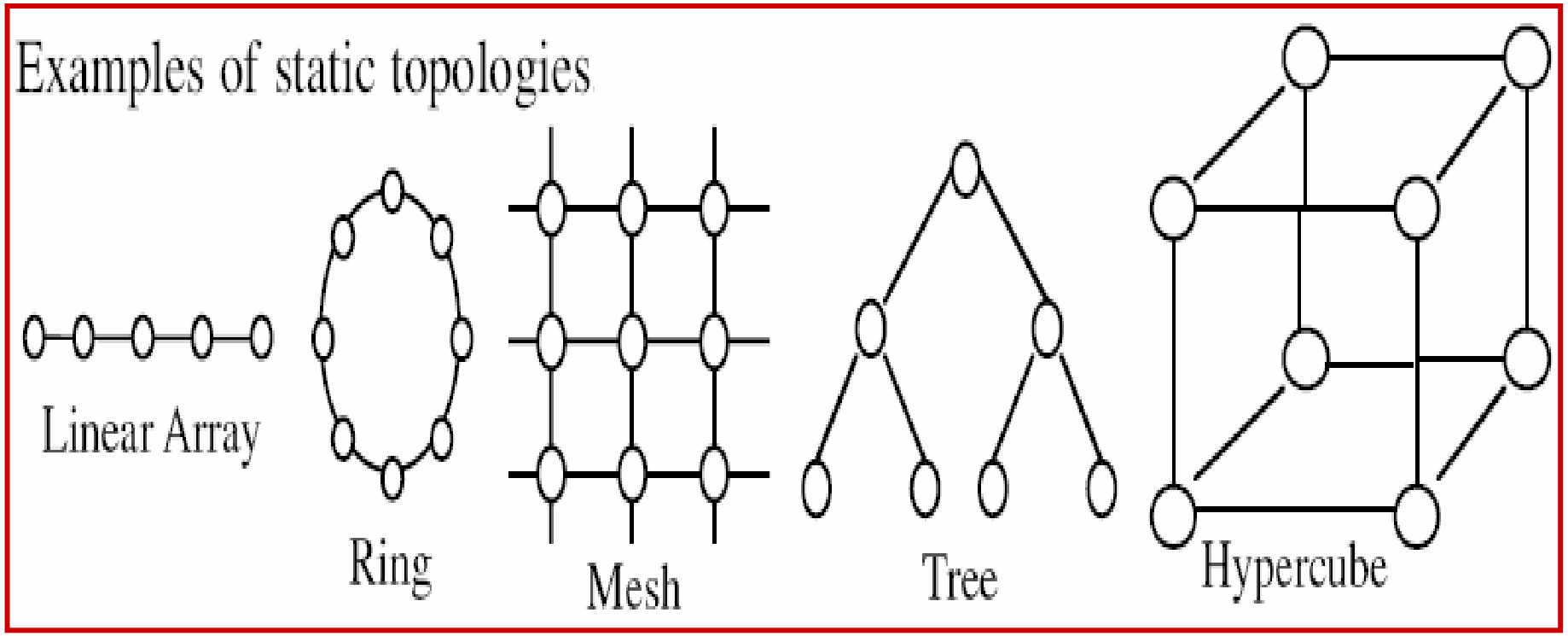


Static & Dynamic INs:

Message passing INs can be divided into static and dynamic.

Static networks form all connections when the system is designed rather than when the connection is needed.

In a static network, messages must be routed along established links.



Dynamic Networks:

Dynamic INs establish a connection between two or more nodes on the fly as messages are routed along the links.

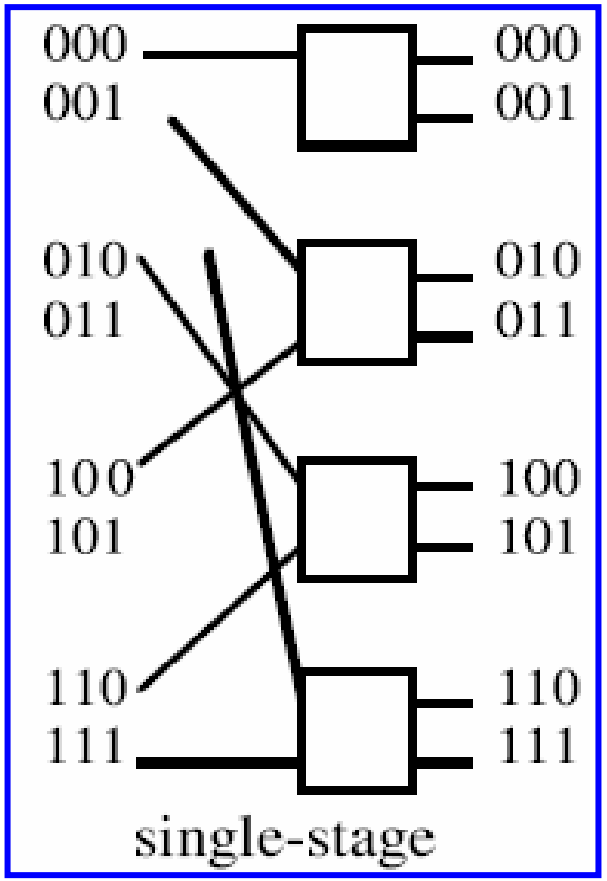
The *number of hops* in a path from source to destination node is equal to the number of point-to-point links a message must traverse to reach its destination.

In either static or dynamic networks, a single message may have to *hop* through intermediate processors on its way to its destination.

The ultimate performance of an interconnection network is greatly influenced by the number of hops taken to traverse the network.

The single-stage interconnection network is a simple dynamic network that connects each of the inputs on the left side to some, but not all, outputs on the right side through a single layer of binary switches represented by the rectangles.

Dynamic INs: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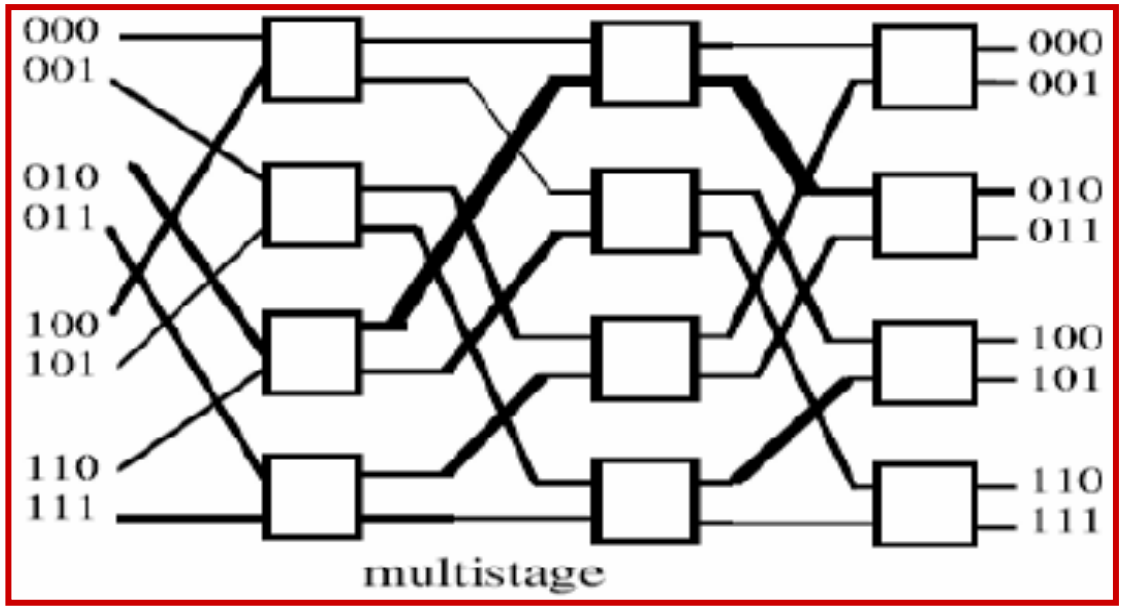
single-stage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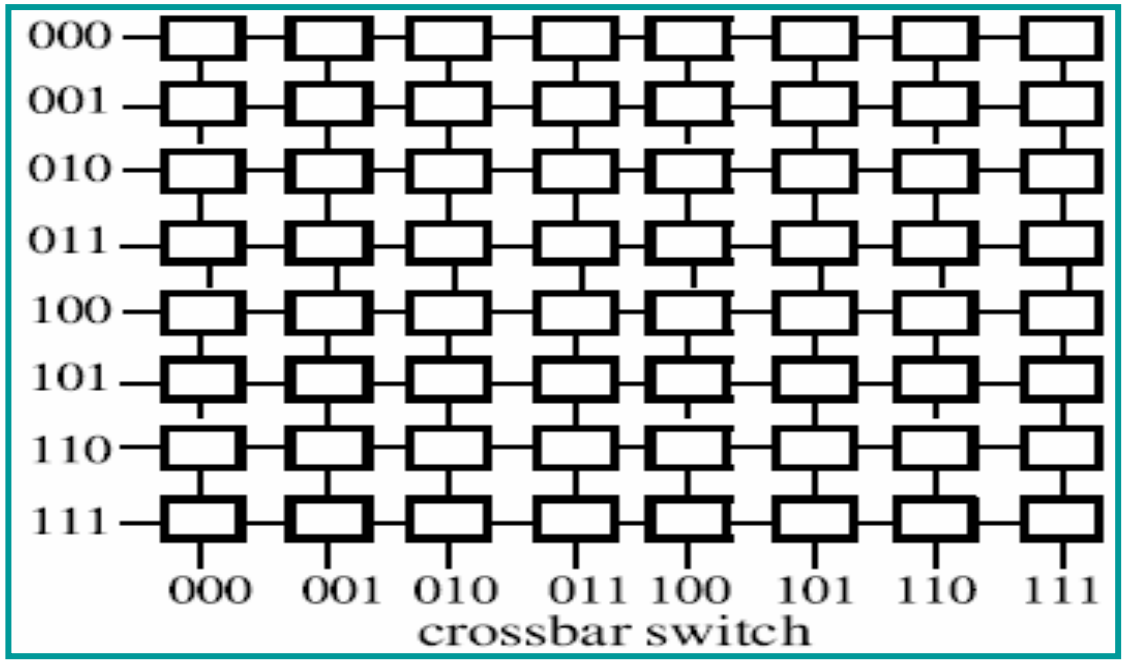
multistage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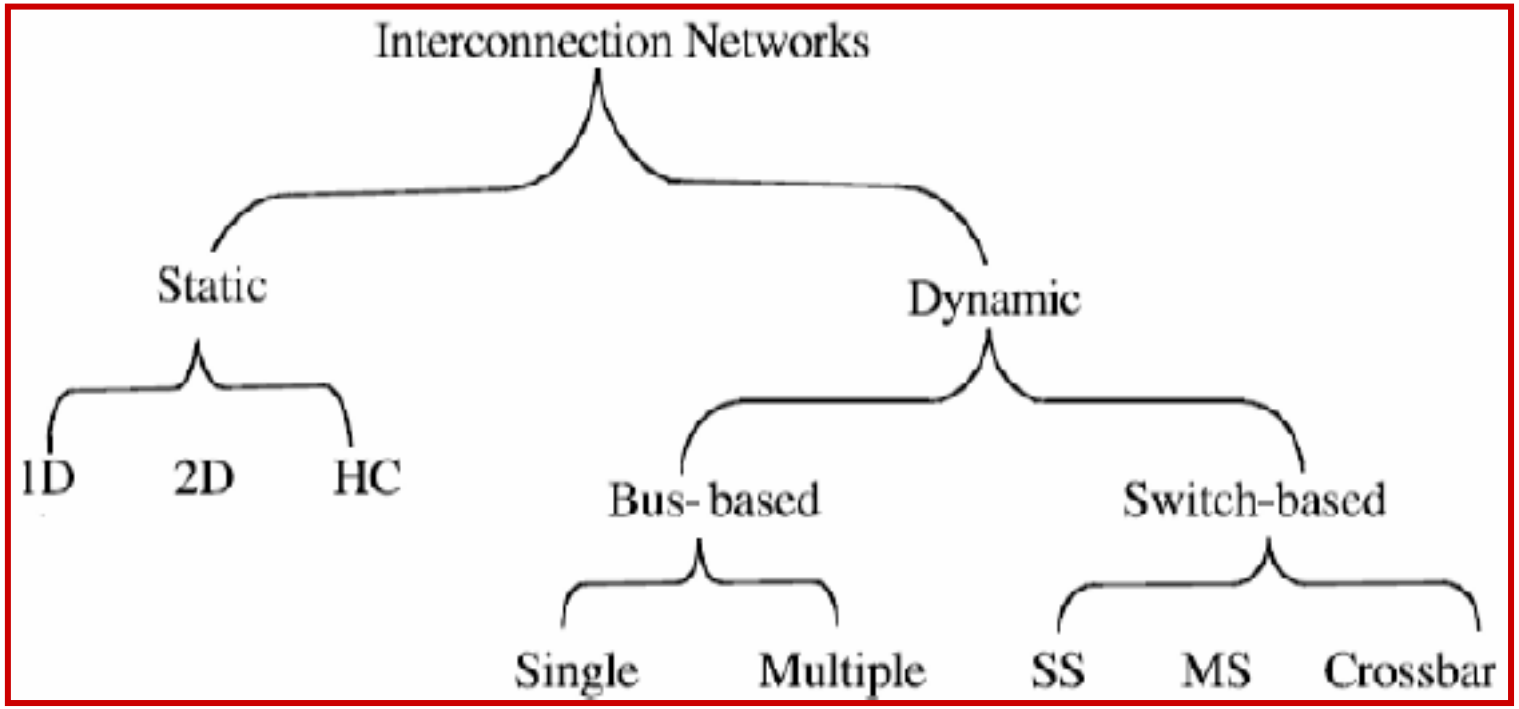
000 001 010 011 100 101 110 111
crossbar switch

INs Taxonomy:

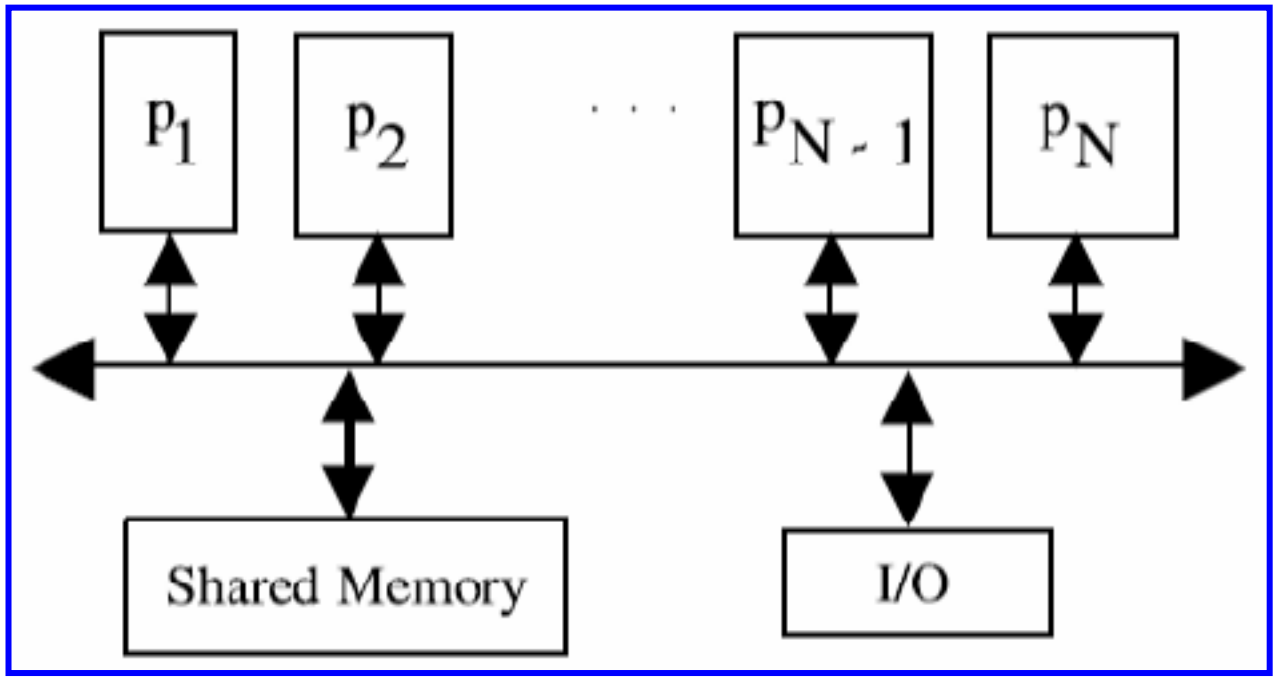
- An IN could be either static or dynamic. Connections in a static network are fixed links, while connections in a dynamic network are established on the fly as needed.
- Static networks can be further classified according to their interconnection pattern as one-dimension (1D), two-dimension (2D), or hypercube (HC).
- Dynamic networks can be classified based on interconnection scheme as bus-based versus switch-based.



BUS-BASED DYNAMIC INs:

Single Bus Systems:

- A single bus is the simplest way to connect MP systems.
- A single bus system consists of N processors, each having its own cache, connected by a shared bus.
- The use of local caches reduces the processor–memory traffic.
- All processors communicate with a single shared memory.



Single Bus Systems Characteristics:

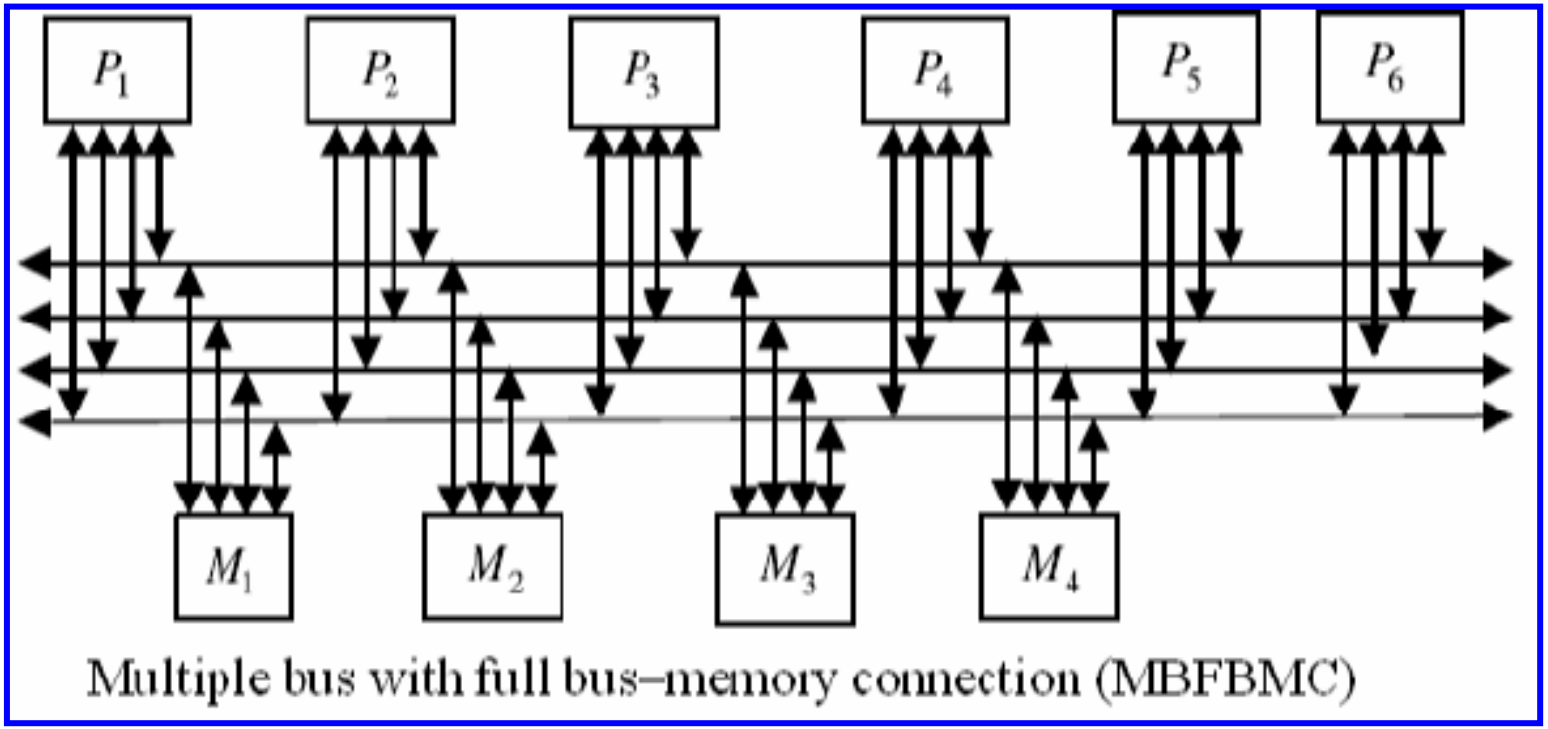
- The typical size of such a system varies between 2 and 50 processors.
- The actual size is determined by the traffic per processor and the bus bandwidth (defined as the maximum rate at which the bus can propagate data once transmission has started).
- The single bus network complexity, measured in terms of the number of buses used, while the time complexity is measured in terms of the amount of input to output delay.
- single bus network is simple and easy to expand.
- Single bus multiprocessors are inherently limited by the bandwidth of the bus and the fact that only one processor can access the bus, and in turn only one memory access can take place at any given time.

Characteristics of Some Commercially Available Single Bus Systems

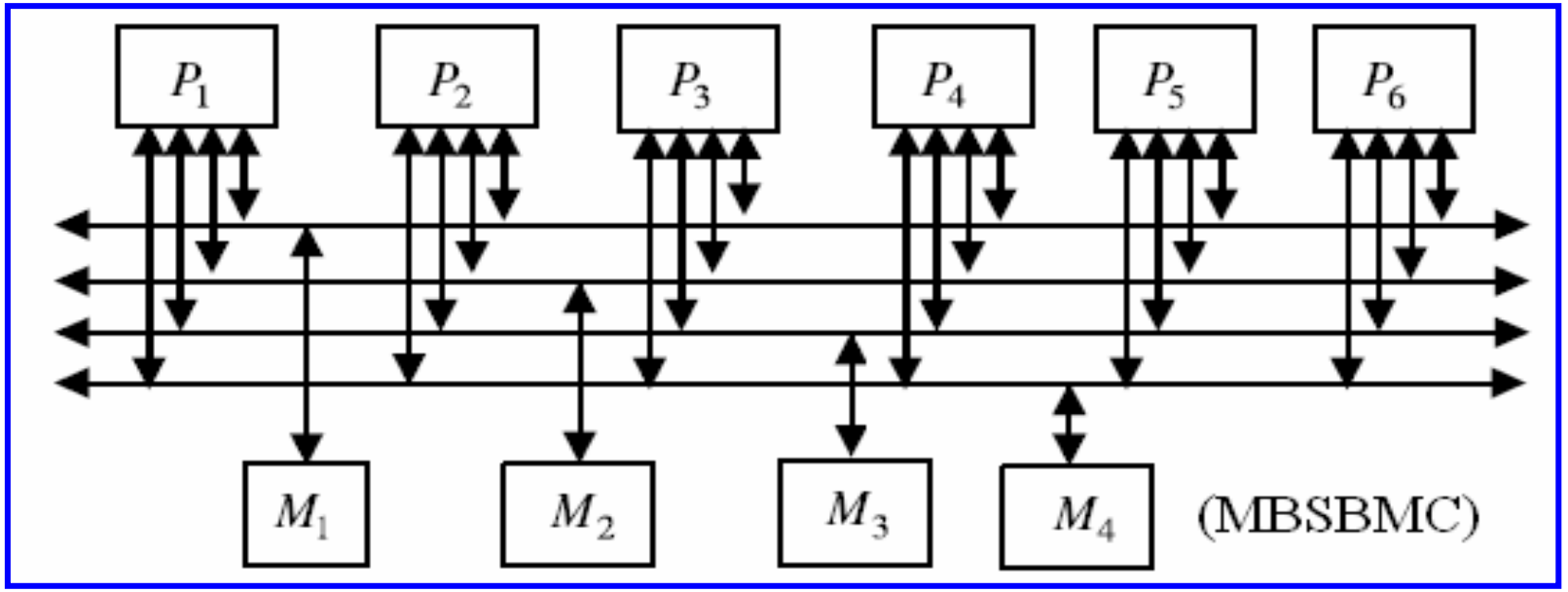
Machine Name	Max No. of Processors	Processor	Clock Rate	Maximum Memory	Bandwidth
HP 9000 K640	4	PA-8000	180 MHz	4,096 MB	960 MB/s
IBM RS/6000 R40	8	PowerPC 604	112 MHz	2,048 MB	1,800 MB/s
Sun Enterprise 6000	30	UltraSPARC 1	167 MHz	30,720 MB	2,600 MB/s

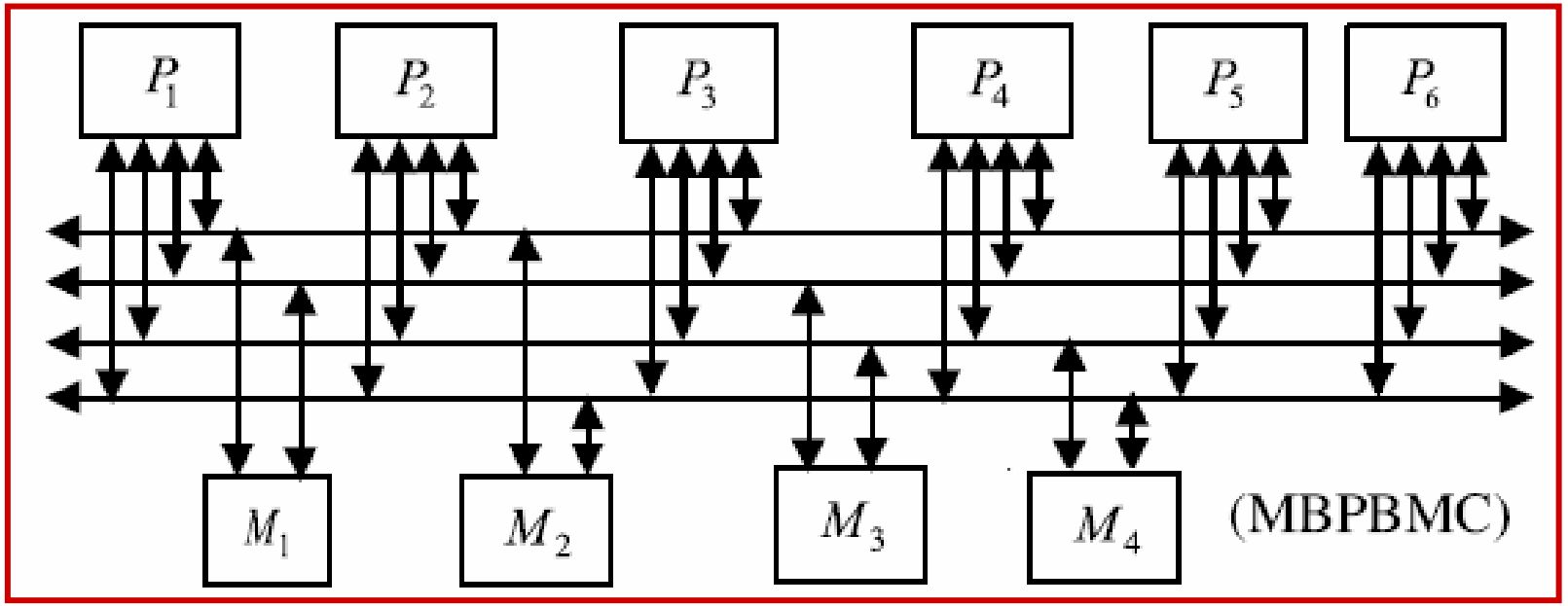
Multiple Bus Systems:

- A multiple bus MP system uses several parallel buses to interconnect multiple processors and multiple memory modules.
- A number of connection schemes are possible in this case:
  - Multiple bus with full bus–memory connection (MBFBMC),
  - Multiple bus with single bus memory connection (MBSBMC),
  - Multiple bus with partial bus–memory connection (MBPBMC),
  - Multiple bus with class-based memory connection (MBCBMC).



Multiple bus with full bus–memory connection (MBFBMC)


P_1
P_2
P_3
P_4
P_5
P_6
M_1
M_2
M_3
M_4
(MBSBMC)


P_1
P_2
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M_1
M_2
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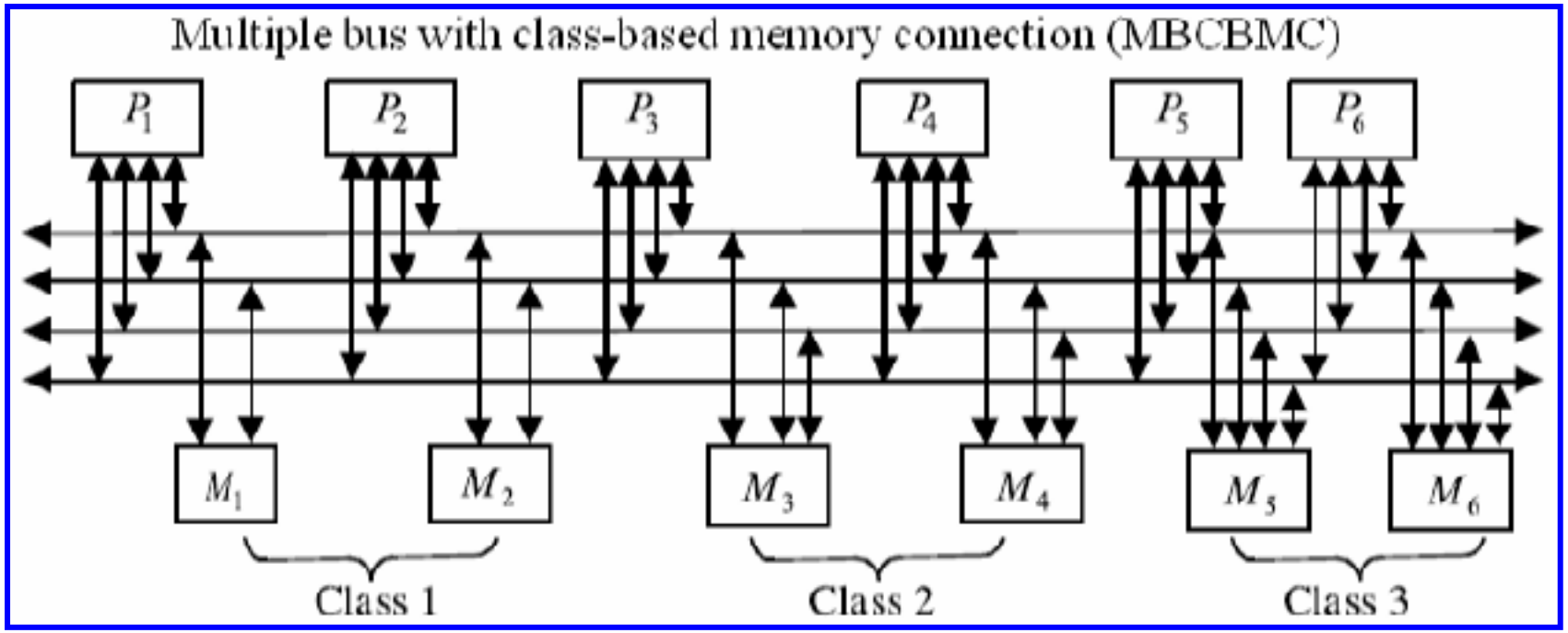
(MBPBMC)



Characteristics of Multiple Bus Architectures

Connection Type	No. of Connections	Load on Bus i
MBFBMC	$B(N+M)$	$N+M$
MBSBMC	$BN+M$	$N+M_j$
MBPBMC	$B(N+M/g)$	$N+M/g$
MBCBMC	$BN+\sum_{j=1}^{k} M_j(j+B-k)$	$N+\sum_{j=\max(i+k-B,1)}^{k} M_j,\ 1 \le i \le B$

Bus Synchronization:

- A bus can be classified as synchronous or asynchronous.
- The time for any transaction over a synchronous bus is known in advance. Asynchronous bus depends on the availability of data and the readiness of devices to initiate bus transactions.
- The process of passing bus mastership from one processor to another is called handshaking and requires the use of two control signals: bus request and bus grant.