Philadelphia University
Faculty of Engineering
Computer Engineering Department

St. Name:
St. Number:

Final Exam, First Semester 2009/2010

Course Title:	**Embedded Systems Design**	**Date:**	26/1/2010
Course No:	0630470	**Time Allowed:**	2 hours
Instructor:	Prof. Kasim Al-Aubidy	**No. of Pages:**	6

Instructions:

- *Write your name and number on each page of the exam.*
- *Consider the **PIC 16F84** Microcontroller running from **8 MHz** crystal frequency.*
- *Use the free space after each assignment for your answer.*
- *Write your answer readable in English.*

Question 1: [25%]

Objectives: Basic concepts of Embedded Systems.

[A]. Choose the correct answer:

1. The baud rate is;
   (a). the total number of bits that can be transmitted.
   (b). the bandwidth of the serial interface.
   (c). the total number of bits per unit time that can be transmitted.
2. CISC processors normally have;
   (a). a large number of general-purpose registers.
   (b). variable instruction length.
   (c). many addressing modes.
3. Each PIC instruction cycle takes
   (a). 2 clock periods. *(b). 4 clock periods.* *(c). single clock period.*
4. The RISC architecture executes most instructions in
   (a). one clock cycle.
   (b). two clock cycles.
   (c). three or more clock cycles.
5. The program counter of the PIC 16F84 is
   (a). 10-bit wide. *(b). 12-bit wide.* *(c). 14-bit wide.*
6. The PIC 16F84 program is stored in a
   (a). flash RAM at address $00C_H$.
   (b). flash RAM at address 000_H.
   (c). flash ROM at address 000_H.
7. To make PortB an output port, you must load register TRISB with
   (a). 80_H *(b). 00_H* *(c). FF_H*
8. To rest the microcontroller if it is ever allowed to overflow use
   (a). reset *(b). sleep* *(c). wdt*

[B]. Embedded systems can be implemented either using single chip microcontrollers or field programmable chips (such as FPGA or FPAA). List the differences between the following:

	Using Microcontroller	Using Field Programmable Chip
1		
2		

	Using FPGA	Using FPAA
1		
2		

[C]. The Harvard structure gives some clear advantages over conventional von Neumann structure. Can you think of any disadvantages? Show that with the help of diagrams?

	Harvard Structure	von Neumann structure
Diagram		
Advantage		
Disadvantage		

Question 2: **[25%]**

Objectives: Basic concepts of Embedded Systems.

[A]. Three microcontrollers (A, B & C) have maximum clock speeds 10MHz, 20MHz, 24MHz respectively. Microcontroller A divides its clock by 4 to give one machine cycle, microcontroller B by 8, and microcontroller C by 12. Microcontrollers A & C take 2 machine cycles to perform an instruction, while microcontroller B takes three cycles.
Place the microcontrollers in order of the speed in which they can perform that instruction?

[B]. If the INTCON register is set to $A8_H$, then

1. Determine which interrupts are enabled?

2. An interrupt occurs, and the INTCON register is found to have changed to $A9_H$, which interrupt source has called?

3. Which bit must the designer change before the end of the ISR, and why?

[C]. A small embedded system has an 8-bit microcontroller requires a regular interrupt every 128 μs.

1. Show how this requirement can be achieved to the best accuracy possible?

	7	6	5	4	3	2	1	0
OPTION Reg								
INTCON Reg								

2. How should the requirement be met if the interrupt is to occur every 500 μs?

	7	6	5	4	3	2	1	0
OPTION Reg								
INTCON Reg								
TMR0 Reg								

Question 3: **[20%]**

Objectives: Microcontroller Programming

[A]. Consider this program:

1. Give the size of sub1?

2. List the changes (Full the table) in the contents of the program counter between the time of execution of the instruction before the call and the instruction following the call?

```
start  EQU   0365
sub1   EQU   079F
start: instruction
       call  sub1
       instruction
         -----
sub1:  instruction 1
       instruction 2
       instruction 3
       instruction 4
       instruction 5
       return
```

PC Contents

[B]. Consider the following delay subroutine:

1. Calculate the delay it actually introduces, taking into account the time taken by every instruction?

```
delay:  movlw   fa
        movwf   delayreg
loop:   nop
        nop
        decfsz  delayreg,1
        goto    loop
        return
```

2. What number should be loaded into delay register to make the generated delay as close as possible to 500μs?

3. Modify the given delay subroutine to introduce a time delay of 10 ms?

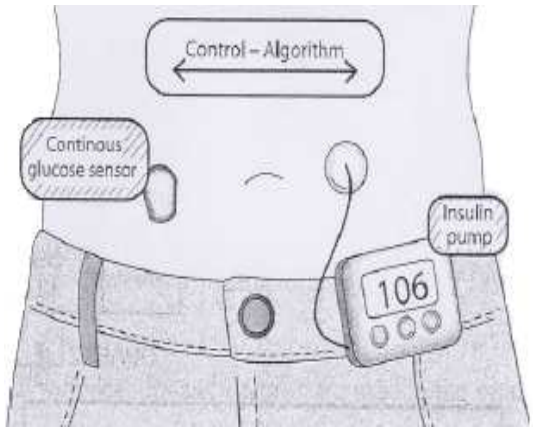
[C]. Outline the procedures of installing a program in the PIC microcontroller during your project design?

Question 4: **[30%]**

Objectives: Hardware and Software Design of an Embedded System

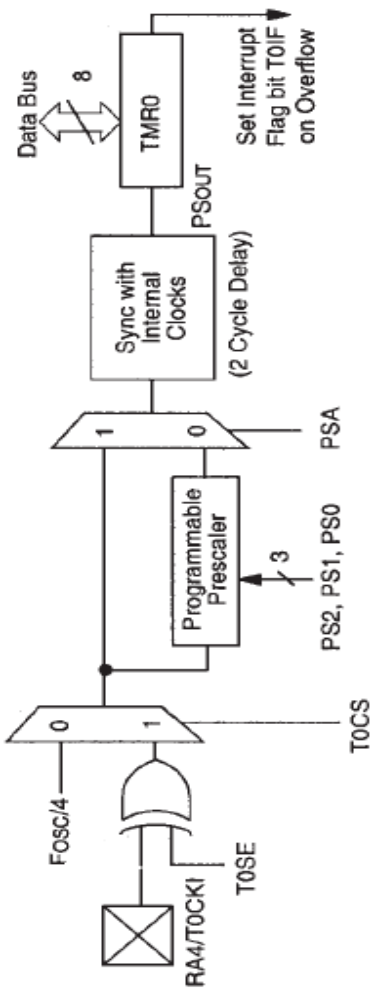
[A]. The counter/timer of the microcontroller is used to measure the speed of an object falling through a column of water. When the object passes an upper sensor the controller starts the counter from zero. When it passes the lower sensor, it stops the counter and reads its value. The microcontroller is clocked from a **1.024** MHz crystal oscillator, and the counter is required to increment every **1 ms**. How should be the **OPTION** register be set?

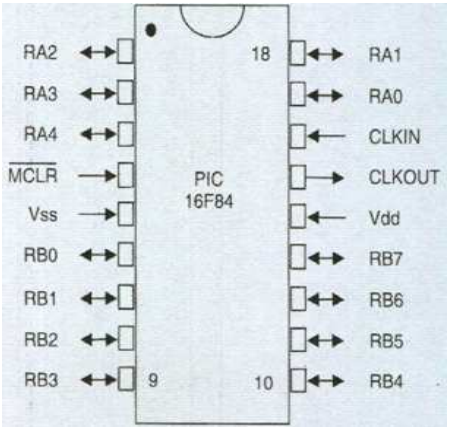
[B]. You have been asked to design an embedded system to regulate glucose levels in the body of someone with diabetes by continuously measuring the level of glucose and dispensing doses of insulin based on those measurements. The chemical glucose sensor generates **4-bit** digital signal. The insulin infusion pump is controlled by a **PWM** signal. The system has **ON/OFF** switch, **RESET** switch, alarm speaker and **LCD** for blood glucose monitoring.



1. Show the general layout of the required system?
2. Give the detailed hardware design of each unit in your design?
3. Draw a flowchart to demonstrate the operation of such a system?
4. If the microcontroller has no enough input/output lines, show how you can interface the LCD serially?

Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSb LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS						
ADDWF	f, d	Add W and f	1	00 0111 dfff ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00 0101 dfff ffff	Z	1,2
CLRF	f	Clear f	1	00 0001 lfff ffff	Z	2
CLRW	-	Clear W	1	00 0001 0xxx xxxx	Z	
COMF	f, d	Complement f	1	00 1001 dfff ffff	Z	1,2
DECF	f, d	Decrement f	1	00 0011 dfff ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1 (2)	00 1011 dfff ffff		1,2,3
INCF	f, d	Increment f	1	00 1010 dfff ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1 (2)	00 1111 dfff ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00 0100 dfff ffff	Z	1,2
MOVF	f, d	Move f	1	00 1000 dfff ffff	Z	1,2
MOVWF	f	Move W to f	1	00 0000 lfff ffff		
NOP	-	No Operation	1	00 0000 0xx0 0000		
RLF	f, d	Rotate Left f through Carry	1	00 1101 dfff ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00 1100 dfff ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00 0010 dfff ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00 1110 dfff ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00 0110 dfff ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS						
BCF	f, b	Bit Clear f	1	01 00bb bfff ffff		1,2
BSF	f, b	Bit Set f	1	01 01bb bfff ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01 10bb bfff ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01 11bb bfff ffff		3
LITERAL AND CONTROL OPERATIONS						
ADDLW	k	Add literal and W	1	11 111x kkkk kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11 1001 kkkk kkkk	Z	
CALL	k	Call subroutine	2	10 0kkk kkkk kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00 0000 0110 0100	$\overline{TO}$,$\overline{PD}$	
GOTO	k	Go to address	2	10 1kkk kkkk kkkk		
IORLW	k	Inclusive OR literal with W	1	11 1000 kkkk kkkk	Z	
MOVLW	k	Move literal to W	1	11 00xx kkkk kkkk		
RETFIE	-	Return from interrupt	2	00 0000 0000 1001		
RETLW	k	Return with literal in W	2	11 01xx kkkk kkkk		
RETURN	-	Return from Subroutine	2	00 0000 0000 1000		
SLEEP	-	Go into standby mode	1	00 0000 0110 0011	$\overline{TO}$,$\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11 110x kkkk kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11 1010 kkkk kkkk	Z	





GIE	EEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	INTCON

IRP	RP1	RP0	TO	PD	Z	DC	C	STATUS

RBPU	INTES	T0CS	T0SE	PSA	PS2	PS1	PS0	OPTION

LCD