# Philadelphia University Faculty of Engineering Computer Engineering Department

Student Name:	
Student Number:	

## Final Exam, First Semester 2007/2008

<b>Course Title:</b>	Embedded Systems Design	Date:	29/1/2008			
Course No:	630470	Time Allowed:	2 hours			
<b>Instructor:</b>	Dr. Kasim Al-Aubidy	No. of Pages:	2			
Question 1:			[20%]			
Objectives: Basic concepts of Embedded Systems.						

Choose the correct answer:

1.	A serial port ada	aptor that receives and trans	smits serial data is calle	ed;
	(a). UART	(b). USART.	(c). $I^2C$ .	(d). SPI.

- 2. The baud rate is;
  - (a). the total number of bits that can be transmitted. (b). the bandwidth of the serial interface.
  - (c). the total number of bits per unit time that can be transmitted. (d). non of the above.
- 3. Flash memory is an economical compromise between EEPROM and EPROM. A high voltage is applied to;
  - (a). selectively erase portions of flash memory. (b). erase the entire block.
  - (c). selectively erase and rewrite portions of flash memory. (d). erase and rewrite the entire block.
- 4. Assembler directives can be used to:
  - (a). improve the hardware design of an embedded system. (b). modify the system reliability.
  - (c). improve the efficiency and flexibility of code production. (d). minimize the size of programs.
- 5. The alphanumeric LCD needs command codes for control operations. It is an;
  - (a) input device receives HEX codes. (b) input device receives ASCII codes.
  - (c). output device receives HEX codes. (d) output device receives ASCII codes.
- 6. After the execution of these instructions "movlw 5A" "andlw A8", the content of WREG is;
- (a). 02. (b). 24. (c). 08. (d). AA. 7. In the PIC16F84 microcontroller, the instruction fetching and execution are done at;
  - (a). the same time. (b). two clock periods. (c). four clock periods. (d). eight clock periods.
- 8. RISC processors normally have;
  - (a) a large number of general-purpose registers. (b). variable instruction length.
  - (c). instructions of variable sizes. (d). many addressing modes.
- 9. The percentage accuracy per bit of a 10-bit ADC at full scale is;
- (a). 0.24%. (b). 0.096%. (c). 0.96%. (d). 0.024%.
- 10. The PIC 16F84 microcontroller has a stack memory with;
- (a). a single-stack level. (b). 2-stack level. (c). 4-stack level. (d). 8-stack level.

## **Question 2:** [30%]

#### Objectives: Embedded Systems Architecture.

- [A]. What is a microcontroller? What are the major differences between microprocessors and microcontrollers?
- [B]. Draw the embedded system design and development model? List FIVE features of the Microcontroller-Based Embedded Systems?
- [C]. The Harvard memory structure gives some clear advantages over conventional von Neumann structure. Can you think of any disadvantages? Show that with the help of diagrams?

**Question 3:** [20%]

# Objectives: Embedded System Programming.

An embedded system has a PIC 16F84 microcontroller with a crystal frequency of 4.0 MHz.

- [A]. Determine the function of the following set of instructions;
- **[B].** Write a 100 msec delay subroutine?

Good Luck

**[C].** The hardware counter/timer (TMR0) of the microcontroller can be used to generate a repetitive interrupts. Explain that and calculate the minimum and maximum interrupt frequency?

adr1:	movlw movwf	value register
adr2:	decfsz	register
	goto	adr2
	return	

<u>Dr. Kasim Al-Aubidy</u>

**Question 4:** [30%]

# Objectives: Microcontroller Interfacing.

Design an embedded system using a suitable microcontroller. The system has an ON/OFF switch, a manual reset switch, 12-button keypad, TWO LEDs to indicate system status, a PWM signal and a direction signal to control the operation of a DC motor.

- 1. Draw the general layout of the embedded system?
- 2. Show the detailed hardware design of the required system?
- 3. Outline a flowchart for the keypad scanning algorithm?
- 4. Explain why a pull-up resistor needed with a switch input?

Mnemonic, Operands			,									
ADDWF			Description	Cycles	MSh	14-Bit	Opcode			Notes	s ∞	terrug it TOI
ADDWF   f, d   Add W and f   f   00 0111 dtff tftf   C,DC,Z   1,2   ADDWF   f, d   AND W with f   f   00 0001 ltff tftf   Z   2,2   2   CLFW   Clear W   f   00 0001 ltff tftf   Z   2,2   2   CLFW   Clear W   f   00 0001 ltff tftf   Z   2,2   2   CLFW   Clear W   f   00 0001 ltff tftf   Z   1,2   2   CLFW   Clear W   f   00 0001 dtff tftf   Z   1,2   2   CLFW   Clear W   f   00 0001 dtff tftf   Z   1,2   2   CLFW   Clear W   f   00 0001 dtff tftf   Z   1,2   2   CLFW   Clear W   f   00 0001 dtff tftf   Z   1,2   2   CLFW   Clear W   f   00 0001 dtff tftf   Z   1,2   2   CLFW   Clear W   C			BYTE-ORIENTED FILE REGIS	TER OPE	1	NS		E30	L			ARO and be and b
ANDWF 1, d AND W with f 1 00 0101 dfff ffff 2 1,2 CLFF f Clear f 1 00 0001 lfff ffff 2 2 2 CLFW - Clear W 1 0 00001 lfff ffff 2 1,2 DECF f, d Decrement f 1 00 1001 dfff ffff 2 1,2 DECF f, d Decrement f 1 00 1001 dfff ffff 2 1,2 DECFSZ f, d Increment f 1 0 10 1001 dfff ffff 2 1,2 INCFSZ f, d Increment f 1 0 10 1001 dfff ffff 2 1,2 INCFSZ f, d Increment f 1 0 0 1001 dfff ffff 2 1,2 INCFSZ f, d Increment f 1 0 0 1001 dfff ffff 2 1,2 INCFSZ f, d Increment f 1 0 0 1000 dfff ffff 2 1,2 INCFSZ f, d Increment f 1 0 0 1000 dfff ffff 2 1,2 INCFSZ f, d Increment f 1 0 0 1000 dfff ffff 2 1,2 INCFSZ f, d Increment f 1 0 0 1000 dfff ffff 2 1,2 INCFSZ f, d Increment f 1 0 0 1000 dfff ffff 2 1,2 INCFSZ f, d Increment f 1 0 0 1000 dfff ffff 2 1,2 INCFSZ f, d Increment f 1 0 0 1000 dfff ffff 2 1,2 INCFSZ f, d Increment f 1 0 0 1000 dfff ffff 2 1,2 INCFSZ f, d Increment f 1 0 0 1000 dfff ffff 1 2 1,2 INCFSZ f, d Increment f 1 0 0 1000 dfff ffff 1 2 1,2 INCFSZ f, d Increment f 1 0 0 1000 dfff ffff fff 2 1,2 INCFSZ f, d Increment f 1 0 0 1000 dfff ffff fff 2 1,2 INCFSZ f, d Increment f 1 0 0 1000 dfff ffff fff 1 1 0 1 0 0 0 0 0 0 0 0 0 0	ADDINE				1				0.00.7		g / \/	₹ NEO
COMF			7 100 77 0010 1	1 :								15
COMF				1 .	1						١ -	T-18
COMF										-	1	1 &
IORWF										1.2		
IORWF											ء ا	= ㅣ뿅
IORWF					1							[ E &   C
IORWF									7		1 1 2	5 등 8   용
IORWF					1						5	150   X
MOVF   f, d		-, -							7		0	
MOVWF   f   Move W to f   1   00   0000   1   1   1   1   1   1												
No Operation										1,46		
RLF		-									/	- S
RRF										1.2	l <del>4                                   </del>	
SUBWF   f, d   Subtract W from f   1   00   0010   defer   feffer   C,DC,Z   1,2   1,2   XORWF   f, d   Swap nibbles in f   1   00   0110   defer   feffer   Z   1,2												
SF									-		1 1	0
SF									0,00,2		1 1	[교교] 있
SF				1 :					7			1881 8
SF	AUTHI	1, 0		ER OPER	-		GLII	1111		1,42	1 1	3 - 3 - 31,
BTFSC   f, b   Bit Set									T		- 1	9.5
BTFSC   f, b   Bit Test f, Skip if Clear   1 (2)   01   10bb   bfff   ffff   3			211 01000 1									E   N
BTFSS   f, b   Bit Test f, Skip if Set   1 (2)   01   11bb   bfff   fffff   3												~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~
LITERAL AND CONTROL OPERATIONS   ADDLW   k   Add literal and W   1   11   111x   kkkk   kkkk   C,DC,Z   ANDLW   k   AND literal with W   1   11   1001   kkkk   kkkk   Z   Z   Z   Z   Z   Z						20 00 10 100					I <b>-</b>	
ANDLW   k	BTFSS	f, b		<del></del>		11bb	bfff	ffff		3	l I	
ANDLW   k				OPERAT	IONS						/ 0	<u> </u>
CALL   k   Call subroutine   2   10   000 k kk k kkk k kkk k kkk k kkk k kkk k kkk k			- 1111 1111 1111 1111 1111							1	Z	
CLRWDT		k							Z		<b> </b>	
GOTO   k   Go to address   2   10   1kkk   kkkk		k		_							/	
MOVLW   k   Move literal to W   1   11   00xx   kkkk   kkkk   kkkk   RETURN   Return from Subroutine   2   00   0000   0000   1000   RETURN   Return from Subroutine   2   00   0000   0000   1000   SLEEP   -   Go into standby mode   1   00   0000   0110   0011   TO,PD   Y		-			0.0	0000			TO,PD		4	$\sim$
MOVLW   k   Move literal to W   1   11   00xx   kkkk   kkkk   kkkk   RETURN   Return from Subroutine   2   00   0000   0000   1000   RETURN   Return from Subroutine   2   00   0000   0000   1000   SLEEP   -   Go into standby mode   1   00   0000   0110   0011   TO,PD   Y		***				30 1-02-03-0				1	8 2	
MOVLW   k   Move literal to W   1   11   00xx   kkkk   kkkk   kkkk   RETURN   Return from Subroutine   2   00   0000   0000   1000   RETURN   Return from Subroutine   2   00   0000   0000   1000   SLEEP   -   Go into standby mode   1   00   0000   0110   0011   TO,PD   Y									Z		l 6	I L #
RETURN   Return with literal in W   2   11   01xx   kkkk   kkkk   RETURN   - Return from Subroutine   2   00   0000   0000   1000   SLEEP   - Go into standby mode   1   00   0000   0110   0011   TO,PD   Y		k										= 8
RETLW   k   Return with illeral in W   2   11   01xx   kkkk   kkkk   kkkk   RETURN   - Return from Subroutine   2   00   0000   0000   1000											_	<u></u>
RETURN -   Return from Subroutine   2   00 0000 0000 1000				_							I \	√ ĕ
SLEEP -   Go into standby mode   1   00 0000 0110 0011   TO,PD       V		-								1	/	<b>√</b> 15
SUBLW k  Subtract W from literal   1   11 110x kkkk kkkk   C,DC,Z     C		-		1								—>' ≴
				1								4
XORLW k Exclusive OR iteral with W 1 11 1010 kkkk kkkk Z	XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z		J	