Embedded Systems Design
(630470)

Lecture 10

Timer/Counter Module

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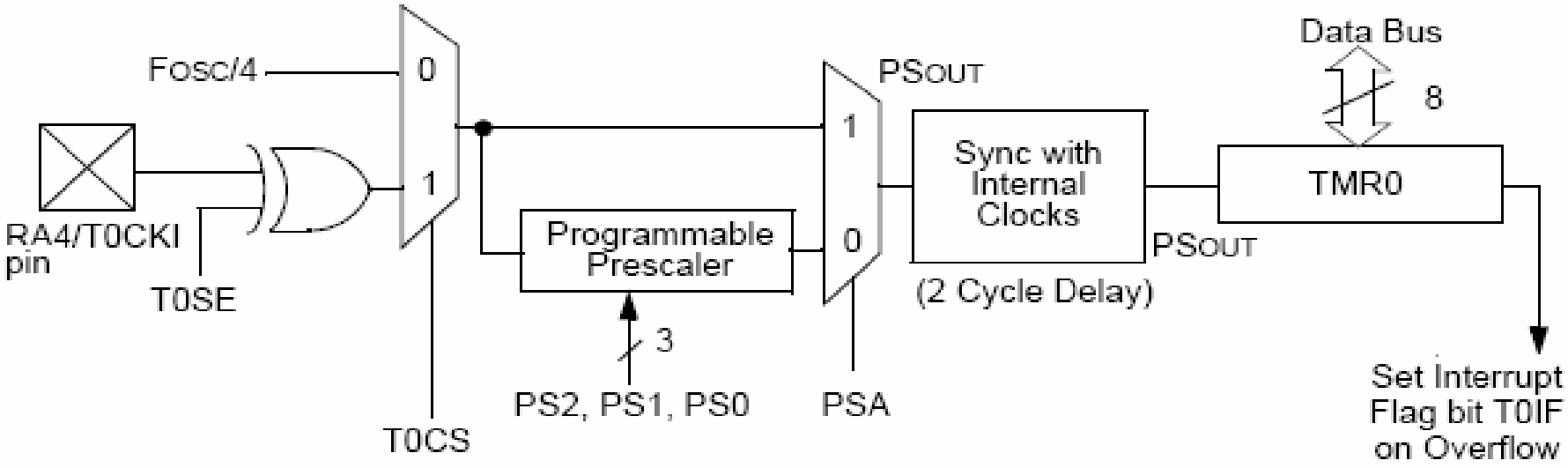
TIMER0 MODULE

- The Timer0 module timer/counter has the following features:
    - 8-bit timer/counter
    - Readable and writable
    - Internal or external clock select
    - Edge select for external clock
    - 8-bit software programmable prescaler
    - Interrupt-on-overflow from FFh to 00h
- Timer0 can operate as a timer or as a counter.

- Timer mode is selected by clearing bit T0CS (OPTION_REG<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler).
- Counter mode is selected by setting bit T0CS (OPTION_REG<5>). In Counter mode, Timer0 will increment, either on every rising or falling edge of pin RA4/T0CKI.

Prescaler

- An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer.
- The PSA and PS2:PS0 bits (OPTION_REG<3:0>) determine the prescaler assignment and prescale ratio.
- Clearing bit PSA will assign the prescaler to the Timer0 module. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, ..., 1:256 are selectable.
- Setting bit PSA will assign the prescaler to the Watchdog Timer (WDT). When the prescaler is assigned to the
- WDT, prescale values of 1:1, 1:2, ..., 1:128 are selectable.
- When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1,etc.) will clear the prescaler.
- When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the WDT



Note: T0CS, T0SE, PSA, PS2:PS0 (OPTION_REG<5:0>).

OPTION REGISTER (ADDRESS 81h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7	**$\overline{\text{RBPU}}$:** PORTB Pull-up Enable bit
bit 6	**INTEDG**: Interrupt Edge Select bit
bit 5	**T0CS**: TMR0 Clock Source Select bit
bit 4	**T0SE**: TMR0 Source Edge Select bit
bit 3	**PSA**: Prescaler Assignment bit
bit 2-0	**PS2:PS0**: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Timer0 Interrupt

- The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h. This overflow sets bit T0IF (INTCON<2>).
- The interrupt can be masked by clearing bit T0IE (INTCON<5>).
- Bit T0IF must be cleared in software by the Timer0 module Interrupt Service Routine before re-enabling this interrupt.
- The TMR0 interrupt cannot awaken the processor from SLEEP since the timer is shut-off during SLEEP.

REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01h	TMR0	Timer0 Module Register							
0Bh,8Bh	INTCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
81h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
85h	TRISA	—	—	—	PORTA Data Direction Register				

Configuration Bits

- The configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations.
- These bits are mapped in program memory location 2007h.
- Address 2007h is beyond the user program memory space and it belongs to the special test/configuration memory space (2000h - 3FFFh). This space can only be accessed during programming.

PIC16F84A CONFIGURATION WORD

R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u
CP	CP	CP	CP	CP	CP	CP	CP	CP	CP	$\overline{\text{PWRTE}}$	WDTE	FOSC1	FOSC0
bit13													bit0

bit 13-4 **CP**: Code Protection bit
1 = Code protection disabled
0 = All program memory is code protected

bit 3 **$\overline{\text{PWRTE}}$**: Power-up Timer Enable bit
1 = Power-up Timer is disabled
0 = Power-up Timer is enabled

bit 2 **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0 **FOSC1:FOSC0**: Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

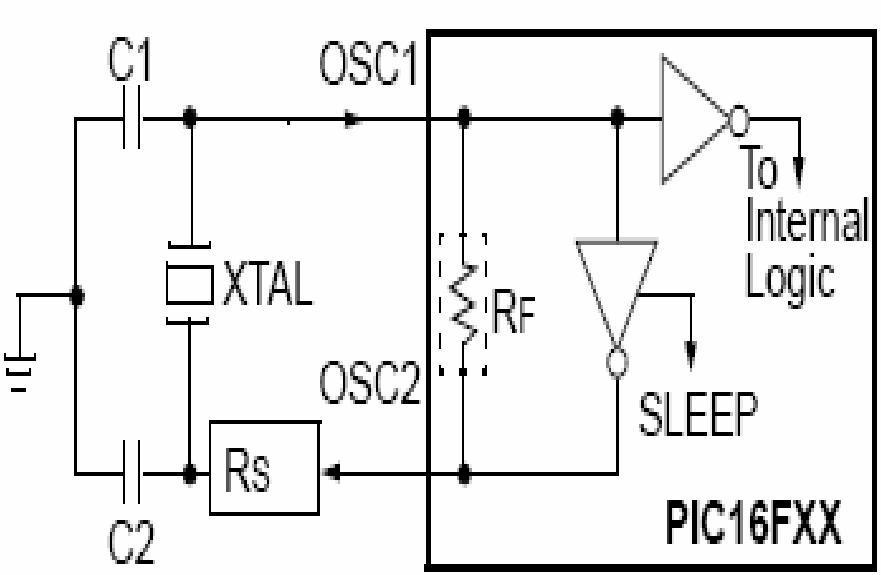
Oscillator Configurations

OSCILLATOR TYPES:

- The PIC16F84A can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:
    - LP Low Power Crystal
    - XT Crystal/Resonator
    - HS High Speed Crystal/Resonator
    - RC Resistor/Capacitor

CRYSTAL OSCILLATOR/ CERAMIC RESONATORS

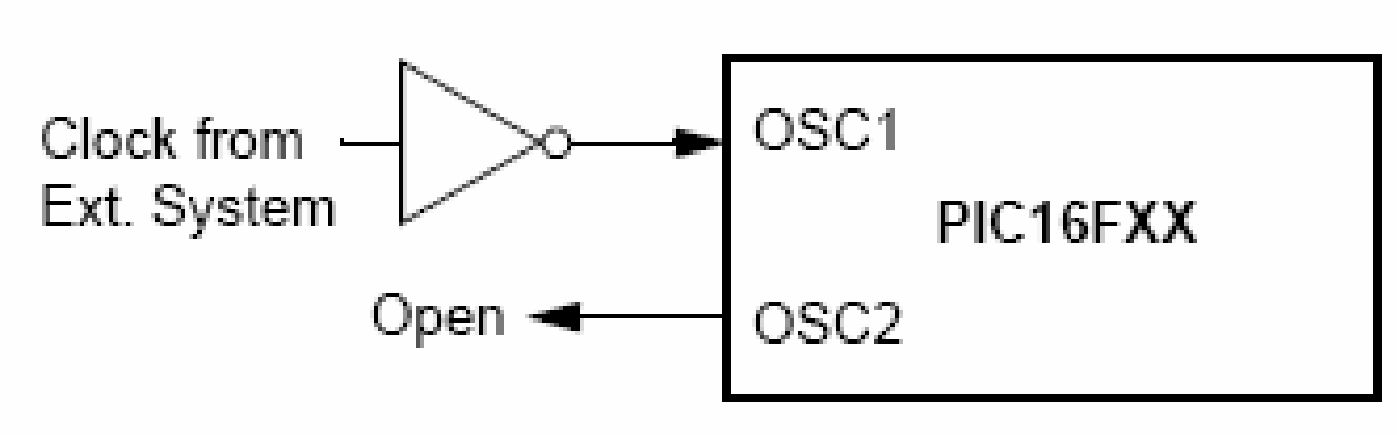
In XT, LP, or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation



Note: A series resistor (RS) may be required for AT strip cut crystals.

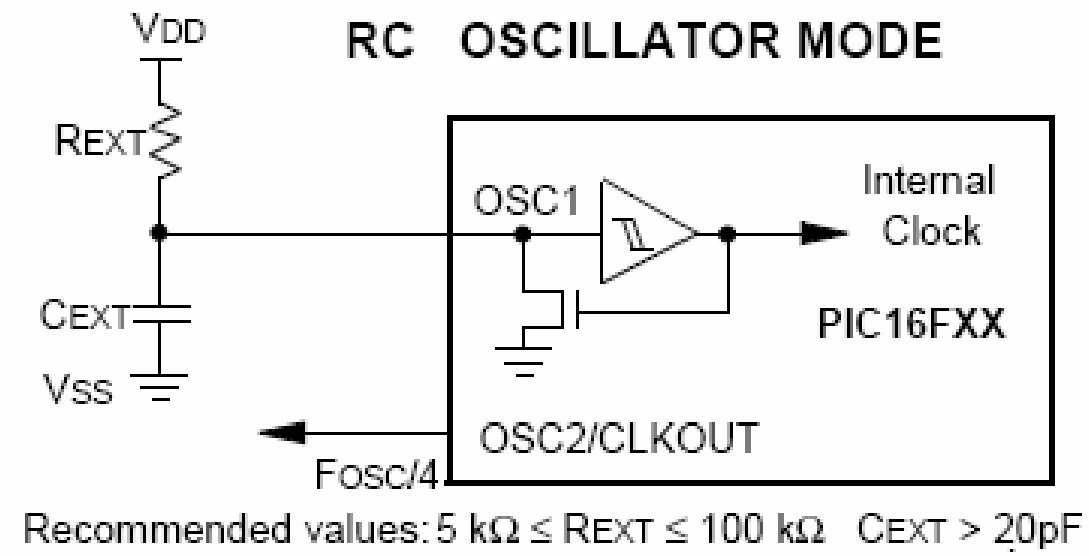
EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

- The PIC16F84A oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP, or HS modes, the device can have an external clock source to drive the OSC1/CLKIN pin



RC OSCILLATOR

- For timing insensitive applications, the RC device option offers additional cost savings.
- The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) values, capacitor (CEXT) values, and the operating temperature.
- The oscillator frequency will vary from unit to unit due to normal process parameter variation.
- The difference in lead frame capacitance between package types also affects the oscillation frequency, especially for low CEXT values.
- The user needs to take into account variation, due to tolerance of the external R and C components.



Recommended values: 5 kΩ ≤ REXT ≤ 100 kΩ CEXT > 20pF