Embedded Systems Design

(630470)

Lecture 9

Input/Output Ports

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- The 16F84 MC has 13 programmable I/O lines (pins).

- Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

PORTA and the TRISA Register

- PORTA is a 5-bit wide, bi-directional port.

- The corresponding data direction register is TRISA.

- Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin.

- The RA4/T0CKI pin is a Schmitt Trigger input and an open drain output.

- All other RA port pins have TTL input levels and full CMOS output drivers.

INITIALIZING PORTA

```
BCF      STATUS, RP0 ;
CLRF     PORTA          ; Initialize PORTA by
                        ; clearing output
                        ; data latches
BSF      STATUS, RP0 ; Select Bank 1
MOVLW    0x0F           ; Value used to
                        ; initialize data
                        ; direction
MOVWF    TRISA          ; Set RA<3:0> as inputs
                        ; RA4 as output
                        ; TRISA<7:5> are always
                        ; read as '0'.
```

PORTA FUNCTIONS

Name	Bit0	Buffer Type	Function
RA0	bit0	TTL	Input/output
RA1	bit1	TTL	Input/output
RA2	bit2	TTL	Input/output
RA3	bit3	TTL	Input/output
RA4/T0CKI	bit4	ST	Input/output or external clock input for TMR0.

SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
05h	PORTA	RA4/T0CKI	RA3	RA2	RA1	RA0
85h	TRISA	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0

PORTB and TRISB Registers

- PORTB is an 8-bit wide, bi-directional port.
- The corresponding data direction register is TRISB.
- Four pins (RB7:RB4) have an interrupt-on-change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupt-on-change comparison).
- The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).
- This interrupt can wake the device from SLEEP.
- The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:
  a) Any read or write of PORTB. This will end the mismatch condition.
  b) Clear flag bit RBIF.

INITIALIZING PORTB

```
BCF      STATUS, RP0 ;
CLRF     PORTB             ; Initialize PORTB by
                           ; clearing output
                           ; data latches
BSF      STATUS, RP0 ; Select Bank 1
MOVLW    0xCF              ; Value used to
                           ; initialize data
                           ; direction
MOVWF    TRISB             ; Set RB<3:0> as inputs
                           ; RB<5:4> as outputs
                           ; RB<7:6> as inputs
```

PORTB FUNCTIONS

Name	Bit	Buffer Type	I/O Consistency Function
RB0/INT	bit0	TTL/ST	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up. Serial programming clock.
RB7	bit7	TTL/ST	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up. Serial programming data.

SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0/INT
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0
81h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
0Bh,8Bh	INTCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF