Philadelphia University
Faculty of Engineering

Student Name:
Student No:

Computer Engineering Department

Quiz Exam, Second Semester: 2010/2011

Course Title: Advanced Computer Architecture	**Date: 2/5/2011**
Course No: 630561	**Time Allowed: 5 minutes**
Instructor: Prof. Kasim Al-Aubidy	**No. of Pages: 1**

Quiz 3: **[5 Marks]**

An instruction pipeline has **FOUR** segments: Fetch **(FI)**, Decode **(DI)**, Execute **(EX)** and WritBack **(WB)**.
Draw the timing diagram of instruction pipeline for:

1. Scalar processor.
2. VLIW computer with super scalar architecture of degree m=3.