Philadelphia University

Faculty of Engineering

Student Name:	
Student Number:	
Serial Number:	

Final Exam, First Semester: 2018/2019
Dept. of Computer Engineering

Course Title:	**Logic Circuits**	**Date:**	03/01/2019
Course No:	**630211**	**Time Allowed:**	2 hours
Lecturer:	Dr. Qadri Hamarsheh	**No. Of Pages:**	7

Instructions:
- **ALLOWED**: pens and drawing tools (**no red color**).
- **NOT ALLOWED**: Papers, calculators, literatures and any handouts. Otherwise, it will lead to the non-approval of your examination.
- **Shut down** Telephones, and other communication devices**.**

Please note:
- *This exam paper contains 6 questions totaling 40 marks*
- *Write your name and your matriculation number on every page of the solution sheets.*
- *All solutions together with solution methods (explanatory statement) must be inserted in the labelled position on the solution sheets.*
- *You can submit your exam after the first hour.*

Basic notions: *The aims of the questions in this part are to evaluate the required minimal student knowledge and skills. Answers in the pass category represent the minimum understanding of basic concepts: Digital Systems, Binary Number Systems, Boolean Algebra, Basic Logic Gates, Boolean Expression Simplification, Karnaugh Maps, and Combinational Sequential Circuits.*

Question 1 **Multiple Choice** ***(10 marks)***

Identify the choice that best completes the statement or answers the question.

1) Which of the following is **not a weighted** value positional numbering system:

a) hexadecimal **b) binary**
c) binary-coded decimal **d) octal**

2) Convert $\mathbf{527_8}$ to binary.

a) 011100111 **b) 101010111**
c) 111010101 **d) 343**

3) The **Gray code** of the binary number **0101** is

a) **1111** **b) 1000**
c) **0111** **d) None of the above**

4) Simplification of the Boolean expression $\boldsymbol{AB + ABC + ABCD + ABCDE + ABCDEF}$ yields which of the following results?

a) $\mathbf{AB}$ **b)** $\mathbf{AB + CD + EF}$
c) $\boldsymbol{ABCDEF}$ **d)** $\mathbf{A + B + C + D + E + F}$

5) Applying **DeMorgan's Law** to $f = \overline{\overline{\overline{AB} + \overline{C}\left(E + \overline{D}\right)}}$ will result in:

a) $f = \overline{A} + \overline{B} + \overline{C} + \overline{E} + D$ **b)** $f = \overline{A}\,\overline{B}\,\overline{C} + E\,\overline{D}$

c) $f = \overline{A}\,\overline{B}\,\overline{C} + (E + \overline{D})$ **d)** $f = \overline{A} + \overline{B} + \overline{C} + \overline{E}D$

6) From the truth table below, determine the standard **SOP** expression.

Inputs			Output
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

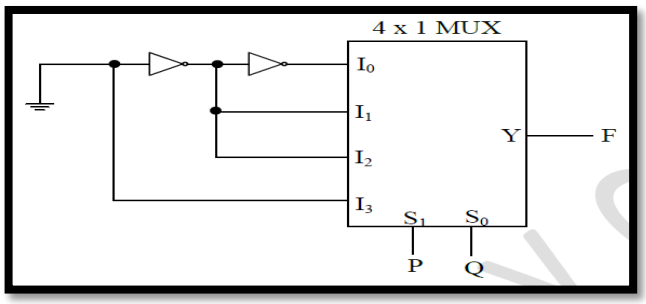
a) $X=\overline{A}\overline{B}C+\overline{A}B\overline{C}+AB\overline{C}$

b) $X=\overline{A}\overline{B}\overline{C}+ABC+A\overline{B}C$

c) $X=ABC+ABC+ABC$

d) $X=A\overline{B}C+\overline{A}BC+AB\overline{C}$

7) The logic function implemented by the circuit below is (ground implies a logic "0")



a) $F = AND\,(P, Q)$ **b)** $F = OR\,(P, Q)$

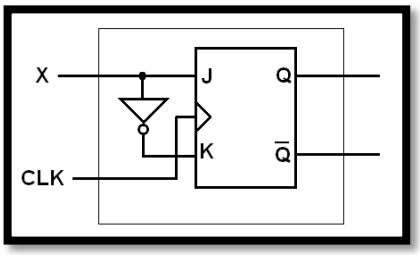
c) $F = XOR\,(P, Q)$ **d)** $F = XNOR\,(P, Q)$

8) The characteristic equation of **S-R** latch is

a) $Q(n+1) = S'R + Q(n)R$ **b)** $Q(n+1) = \big(S + Q(n)\big)R'$

c) $Q(n+1) = SR + Q(n)R$ **d)** $Q(n+1) = S'R + Q'(n)R$

9) The figure shown below is -------



a) **A T flip flop** **b)** **An S-R latch**

c) **A JK flip flop** **d)** **A D flip flop**

10) A **ripple counter** is a(n) ---------- device

a) **asynchronous** **b)** **Combinational**

c) **synchronous** **d)** **None of them**

Question 2 ***(6 marks)***

a) Prove the identity of the following Boolean equation, using **algebraic manipulation**: ***(2 marks)***

$$\overline{A}B + \overline{B}\overline{C} + AB + \overline{B}C = 1$$

Solution

b) Draw **4-bit asynchronous** binary **counter** using **JK** flip flops and its **timing diagram**. ***(4 marks)***

Solution

Familiar and Unfamiliar Problems Solving: *The aim of the questions in this part is to evaluate that the student has some basic knowledge of the key aspects of the lecture material and can attempt to solve familiar and unfamiliar problems of Combinational and Sequential Circuits and Analysis of Sequential Circuits.*

Question 3 Implement **full adder** circuit using **4:1 multiplexers**. ***(4 marks)***

Solution

Question 4 *(7 marks)*

The **1-bit full subtractor** shown in the following figure performs the binary subtraction

$$\boldsymbol{P - Q - B_{in}}$$

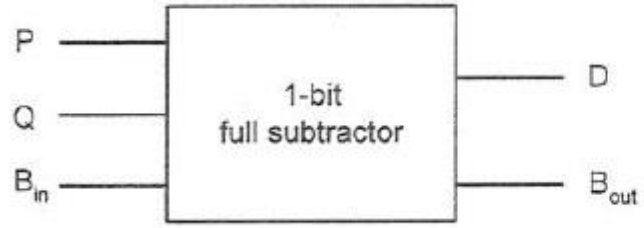
Where **P** and **Q** are 1-bit variables and $\boldsymbol{B_{in}}$ is borrow input from the previous stage. It produces two outputs: the difference **D** and the borrow output $\boldsymbol{B_{out}}$. The truth table describing the function of this 1-bit full subtractor is shown in table.

Do the following:

a) Derive the Boolean expressions for **D** and $\boldsymbol{B_{out}}$ using **K-map**. *(3 marks)*

b) Implement **D** and $\boldsymbol{B_{out}}$ **logic circuits**. *(2 marks)*

c) Design the 1-bit full subtractor using **3x8 decoder**. *(2 marks)*

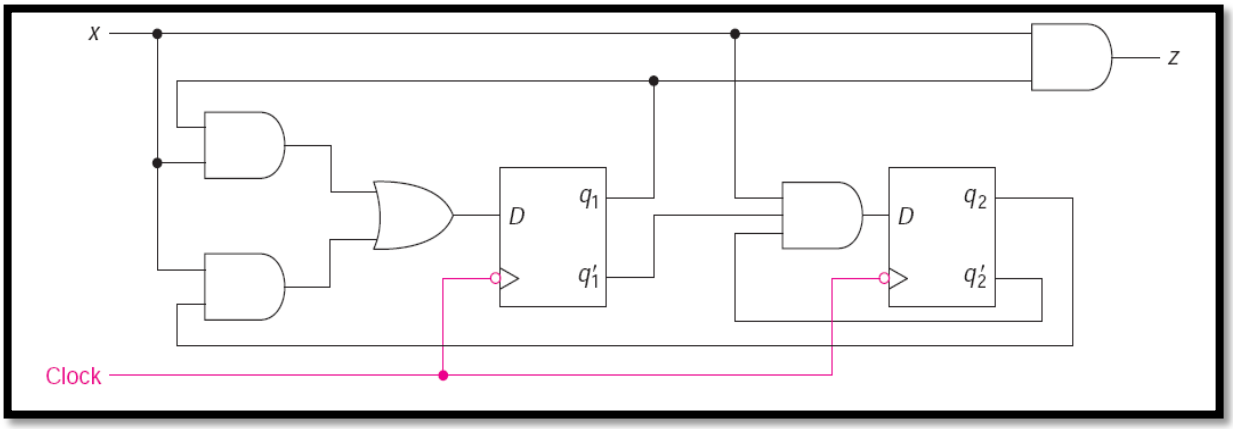


B_{in}	P	Q	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

Solution

Question 5 ***(6 marks)***

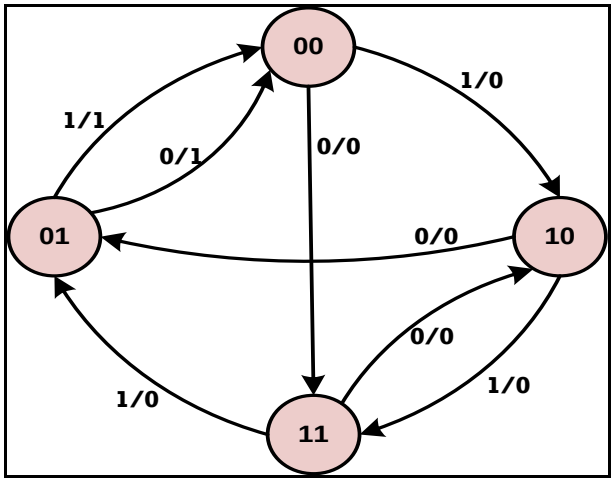
- Derive the **Next-state and Output equations, Next-state table,** and draw the **state diagram** for the sequential circuit shown in the following figure. There is **one input, x**, and **one output, z.**



Solution

Question 6 *(7 marks)*

Given the following **state diagram**, design a clocked sequential circuit using **JK flip-flops**.



Solution

GOOD LUCK