Philadelphia University

Faculty of Engineering

Student Name:
Student Number:
Serial Number:

Final Exam, Second Semester: 2018/2019
Dept. of Computer Engineering

Course Title:	**Logic Circuits**	**Date:**	02/06/2019
Course No:	**630211**	**Time Allowed:**	2 hours
Lecturer:	Dr. Qadri Hamarsheh	**No. Of Pages:**	8

Instructions:

- **ALLOWED**: pens and drawing tools (**no red color**).
- **NOT ALLOWED**: Papers, calculators, literatures and any handouts. Otherwise, it will lead to the non-approval of your examination.
- **Shut down** Telephones, and other communication devices**.**

Please note:

- *This exam paper contains 6 questions totaling 40 marks*
- *Write your name and your matriculation number on every page of the solution sheets.*
- *All solutions together with solution methods (explanatory statement) must be inserted in the labelled position on the solution sheets.*
- *You can submit your exam after the first hour.*

Basic notions: *The aims of the questions in this part are to evaluate the required minimal student knowledge and skills. Answers in the pass category represent the minimum understanding of basic concepts: Digital Systems, Binary Number Systems, Boolean Algebra, Basic Logic Gates, Boolean Expression Simplification, Karnaugh Maps, Combinational and Sequential Circuits.*

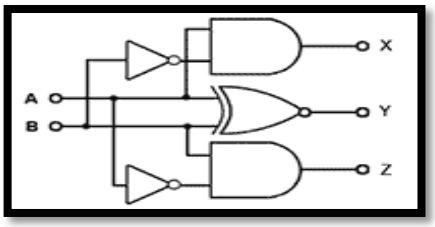
Question 1 **Multiple Choice** ***(10 marks)***

Identify the choice that best completes the statement or answers the question.

1) The binary number **11101011000111010** can be written in hexadecimal as _____.

a) $\mathbf{DD63A_{16}}$ **b)** $\mathbf{1D63A_{16}}$
c) $\mathbf{1D631_{16}}$ **d)** $\mathbf{1D33A_{16}}$

2) Refer to the following figure. If **A = 0** and **B = 1**, what will be the logic states at **X, Y** and **Z**?



a) **X=1, Y=1, Z=0** **b)** **X=1, Y=0, Z=0**
c) **X=0, Y=0, Z=1** **d)** **X=0, Y=1, Z=0**

3) The **simplification** of the Boolean expression $\left(\overline{A\bar{B}\bar{C}}\right) + \left(\overline{A\bar{B}C}\right)$ is

a) **0** **b)** **1**
c) **A** **d)** **BC**

4) The **equivalent canonical (standard) form** for the following logical expression

$$\mathbf{F = AB + C}$$ is

a) $\mathbf{F = ABC + \bar{A}BC + A\bar{B}C + \bar{A}\bar{B}C}$
b) $\mathbf{F = ABC + A\bar{B}C + \bar{A}\bar{B}C + AB\bar{C}}$
c) $\mathbf{F = ABC + \bar{A}BC + A\bar{B}C + \bar{A}\bar{B}C + AB\bar{C}}$
d) **None of the above**

5) The function $\mathbf{F(A,B,C)} = \sum(\mathbf{1,2,3,5,7})$ is equivalent to

a) $\overline{C} + \overline{A}B$ **b)** $C + AB$

c) $C + \overline{A}B$ **d)** $C + A\overline{B}$

6) Which of the following circuits come under the class of combinational logic circuits?

1. Full adder **2.** Full subtracter

3. Half adder **4.** J-K flip

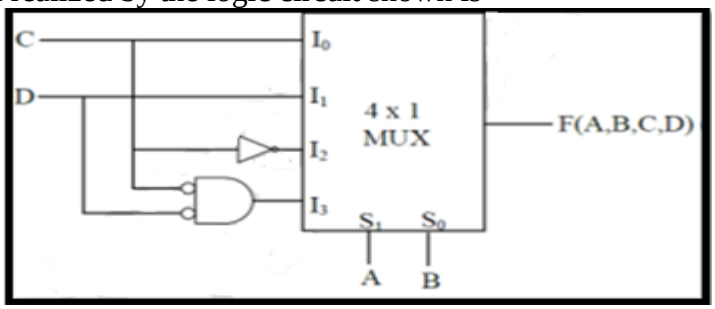
5. Counter

Select the correct answer from the codes given below:

a) **1 only** **b)** **3 and 4**

c) **4 and 5** **d)** **1, 2, and 3**

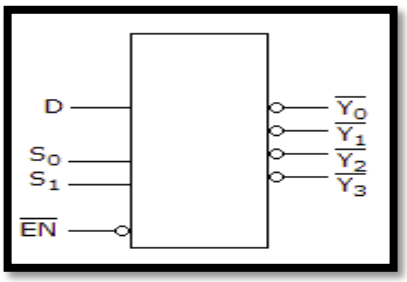
7) The Boolean function realized by the logic circuit shown is



a) $\mathbf{F = \Sigma m\,(0,1,3,5,9,10.14)}$ **b)** $\mathbf{F = \Sigma m\,(2,3,5,7,8,12.13)}$

c) $\mathbf{F = \Sigma m\,(1,2,4,5,11,14.15)}$ **d)** $\mathbf{F = \Sigma m\,(2,3,5,7,8,9.12)}$

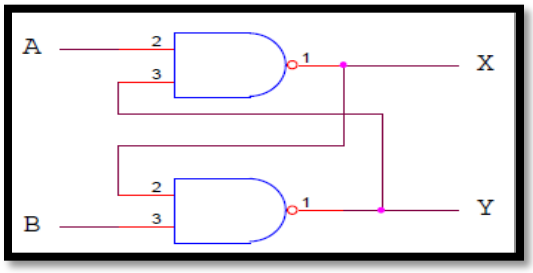
8) The circuit shown here is most likely a _____.



a) **Adder** **b)** **Multiplexer**

c) **Demultiplexer** **d)** **Parity generator**

9) If the input combination **A=0, B=1** is applied to this circuit, the (steady state) output will be:



a) **X=0, Y=0** **b)** **X=0, Y=1**

c) **X=1, Y=0** **d)** **X=1, Y=1**

10) The characteristic equation for the **T**-Flip Flop is:

a) $Q(t+1) = T.\overline{Q} + \overline{T}.Q$ **b)** $Q(t+1) = \overline{T}.\overline{Q} + T.Q$

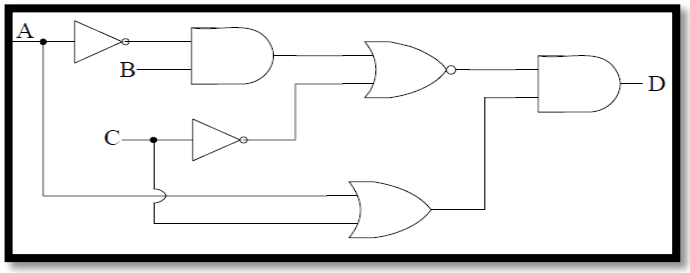
Familiar and Unfamiliar Problems Solving: *The aim of the questions in this part is to evaluate that the student has some basic knowledge of the key aspects of the lecture material and can attempt to solve familiar and unfamiliar problems of Combinational and Sequential Circuits and Analysis of Sequential Circuits.*

Question 2 ***(6 marks)***

a) List three **weighted Binary codes**. ***(1.5 marks)***

Solution

b) For the following logic circuit, find $\mathbf{D = f(A, B, C)}$, that is, express the output **D** in terms of the inputs **A, B** and **C**, **simplify** the Boolean expression obtained, and **draw** the circuit. ***(2.5 marks)***



Solution

c) Express the function ***(2 marks)***

$$D = f(A, B, C) = A + \overline{B}C$$

in a **sum of minterms** form.

Solution

Question 3 ***(7 marks)***

a) Construct the **full adder** using **two half adders** (use **XOR** gates) and one **OR** gate (you must proof your answer with the help of equations). ***(4 marks)***

Solution

b) Give the **Characteristic equations** and the **Excitation tables** for the SR and JK flip-flops. ***(3 marks)***

Solution

Question 4 ***(7 marks)***

a) A combinatorial circuit is defined by the following three Boolean functions: ***(3 marks)***

$$F1 = \overline{(X + Z)} + XYZ$$
$$F2 = \overline{(X + Z)} + \bar{X}YZ$$
$$F3 = X\bar{Y}Z + \overline{(X + Z)}$$

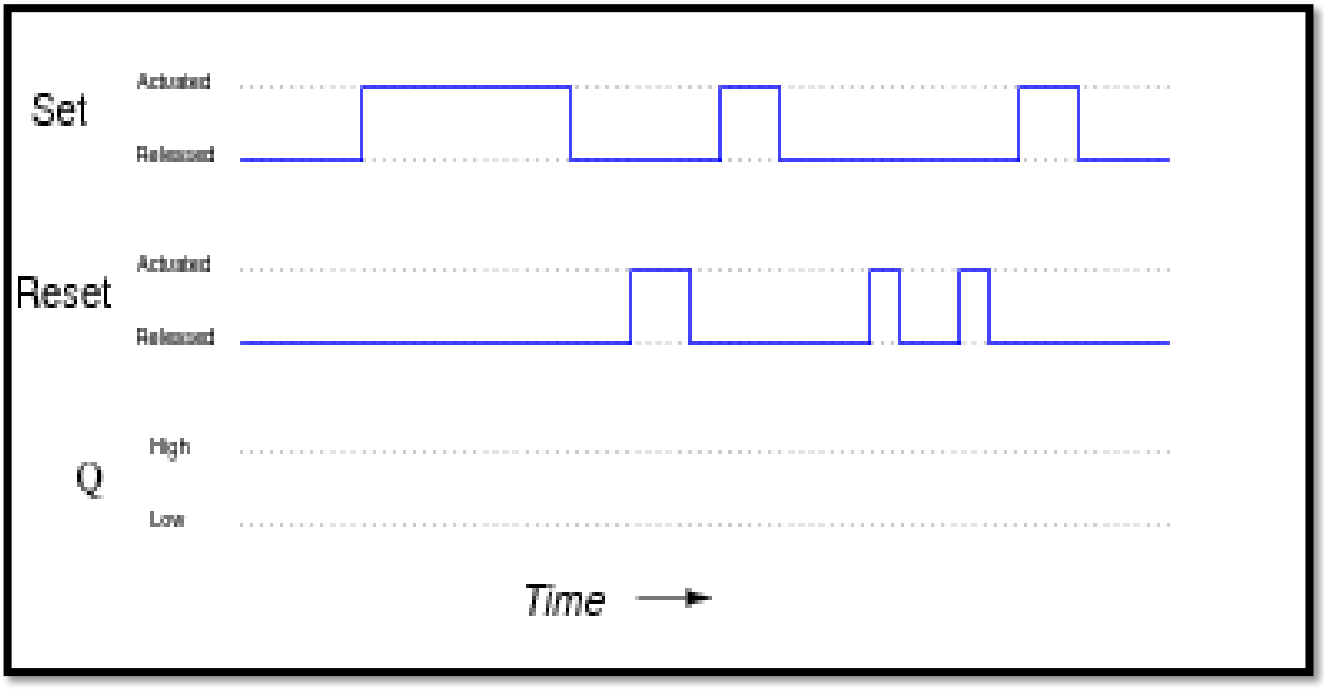
Design a circuit with a single **decoder** and external **OR** gates.

Solution

b) Design a **32-to-1** multiplexer using only **8-to-1** multiplexer. Use **block diagram** for the components. ***(2 marks)***

Solution

c) Complete the **timing diagram**, showing the state of the **Q** output over time as (**SR Latch**) the **Set** and **Reset** switches are actuated. Assume that **Q** begins in the **low state**: ***(2 marks)***



Question 5 ***(5 marks)***

A sequential circuit with two **D** Flip-Flops, **A** and **B**; two inputs, **x** and **y**; and one output, **z**, is specified by the following **next-state** and **output equations**:

$$A(t+1) = \bar{x}y + xA$$
$$B(t+1) = \bar{x}B + xA$$
$$z = B$$

a) **Draw** the circuit. ***(1.5 marks)***

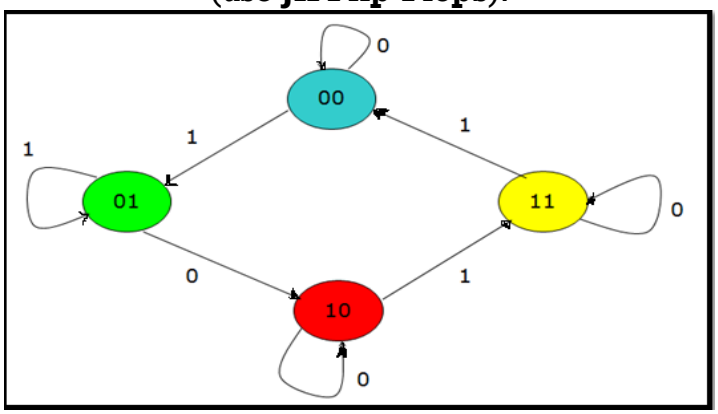
b) List the **state table** for the sequential circuit. ***(2 marks)***

c) Draw the corresponding **state diagram**. ***(1.5 marks)***

Solution

Question 6 ***(5 marks)***

Design a **clocked sequential** circuit that operates according to the following **state diagram** (use **JK Flip-Flops**).



Solution

GOOD LUCK