Philadelphia University

Faculty of Engineering

Student Name:	
Student Number:	
Serial Number:	

Final Exam, First Semester: 2019/2020
Dept. of Computer Engineering

Course Title:	**Logic Circuits**	**Date:**	28/01/2020
Course No:	**630211**	**Time Allowed:**	2 hours
Lecturer:	Dr. Qadri Hamarsheh	**No. Of Pages:**	8

Instructions:

- **ALLOWED**: pens and drawing tools (**no red color**).
- **NOT ALLOWED**: Papers, calculators, literatures and any handouts. Otherwise, it will lead to the non-approval of your examination.
- **Shut down** Telephones, and other communication devices**.**

Please note:

- *This exam paper contains 6 questions totaling 40 marks*
- *All solutions together with solution methods (explanatory statement) must be inserted in the labelled position on the solution sheets.*

Basic notions: *The aims of the questions in this part are to evaluate the required minimal student knowledge and skills. Answers in the pass category represent the minimum understanding of basic concepts: Digital Systems, Binary Number Systems, Boolean Algebra, Basic Logic Gates, Boolean Expression Simplification, Karnaugh Maps, Combinational and Sequential Circuits.*

Question 1 **Multiple Choice** ***(10 marks)***

Identify the choice that best completes the statement or answers the question.

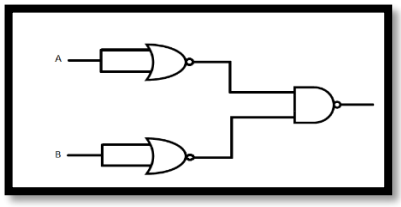
1) The **binary** number **101110101111010** can be written in **octal** as _____.

a) 51562_8 **b)** 56577_8
c) 56572_8 **d)** 65627_8

2) The **excess-3** code of decimal number **26** is:

a) **01001101** **b)** **01001001**
c) **10001001** **d)** **01011001**

3) In the circuit shown below, which logic function does this circuit generate?



a) **OR** **b)** **AND**
c) **NOR** **d)** **NAND**

4) The **dual** of the Boolean function $x + yz$ is:

a) $\bar{x}(\bar{y} + \bar{z})$ **b)** $x(y + z)$
c) $x + yz$ **d)** $\bar{x} + \bar{y}\bar{z}$

5) Applying **DeMorgan's theorem to** the expression $\overline{\overline{(X + Y)} + \bar{Z}}$, we get _____

a) $(X+Y)Z$ **b)** $(\bar{X}+\bar{Y})\bar{Z}$
c) $(\bar{X}+\bar{Y})Z$ **d)** $(X+Y)\bar{Z}$

6) The K-map for a Boolean function is shown in the figure. The number of **essential prime implicants** for this function is

CD \ AB	00	01	11	10
00	1	1	0	1
01	0	0	0	1
11	1	0	0	0
10	1	0	0	1

a) 4 **b) 5**
c) 6 **d) 8**

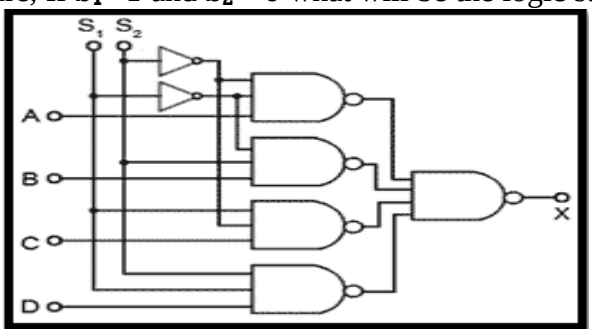
7) **Any** combinational circuit can be built using

1. *NAND gates.* 2. *NOR gates.*
3. *EX-OR gates.* 4. *Multiplexers.*

Which of these are correct?

a) 1, 2 and 3 **b) 1, 3 and 4**
c) 2, 3 and 4 **d) 1,2 and 4**

8) Refer to the following figure, If **S_1=1** and **S_2= 0** what will be the logic state at the output **X**?



a) X = A **b) X = B**
c) X = C **d) X = D**

9) **PRESET** and **CLEAR** inputs are normally **synchronous**.

a) True **b) False**

10) When designing the circuit with the state table shown below using **JK** flip flops, then **J_A**=..., **K_A**=….

Present State		Input	Next State		JA	KA
A	B	X	A	B		
0	0	0	0	0		
0	0	1	0	1		
0	1	0	1	0		
0	1	1	0	1		
1	0	0	1	0		
1	0	1	1	1		
1	1	0	1	1		
1	1	1	0	0		

a) $J_A = B'.x', K_A = A'$ **b) $J_A = B.x , K_A = A$**
c) $J_A = B\,X , K_A = A'$ **d) $J_A = B.x' , K_A = B.x$**

Familiar and Unfamiliar Problems Solving: *The aim of the questions in this part is to evaluate that the student has some basic knowledge of the key aspects of the lecture material and can attempt to solve familiar and unfamiliar problems of Combinational and Sequential Circuits and Analysis of Sequential Circuits.*

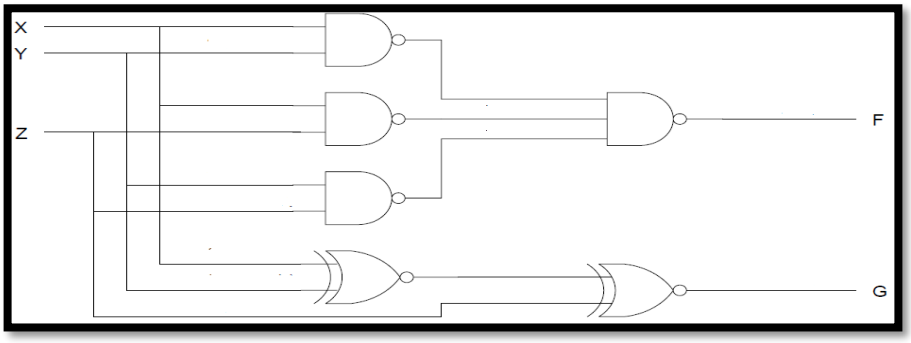
Question 2 ***(6 marks)***

a) Simplify the Boolean expression using **Boolean algebra**. ***(2 marks)***

$$(a.b.(c+\overline{b.d})+\overline{a.b}).c.d$$

Solution

b) The logic circuit below has three inputs, ***X, Y***, and ***Z***, and two outputs, ***F*** and ***G***. **Find** the **minterm** list and **maxterm** list representations for the outputs ***F*** and ***G***. ***(4 marks)***



Solution

Question 3 ***(6 marks)***

Using the following table (**Binary Code and Gray Code**), do the following:

Design a **Binary-to-Gray code converter** using any available method to minimize the logic and implement the logic circuit using **XOR circuits**.

Binary Code				Gray Code			
B3	**B2**	**B1**	**B0**	**G3**	**G2**	**G1**	**G0**
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

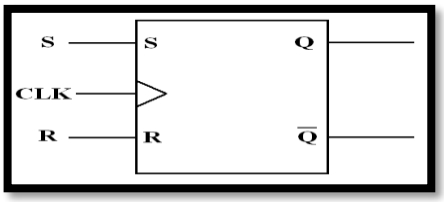
Solution

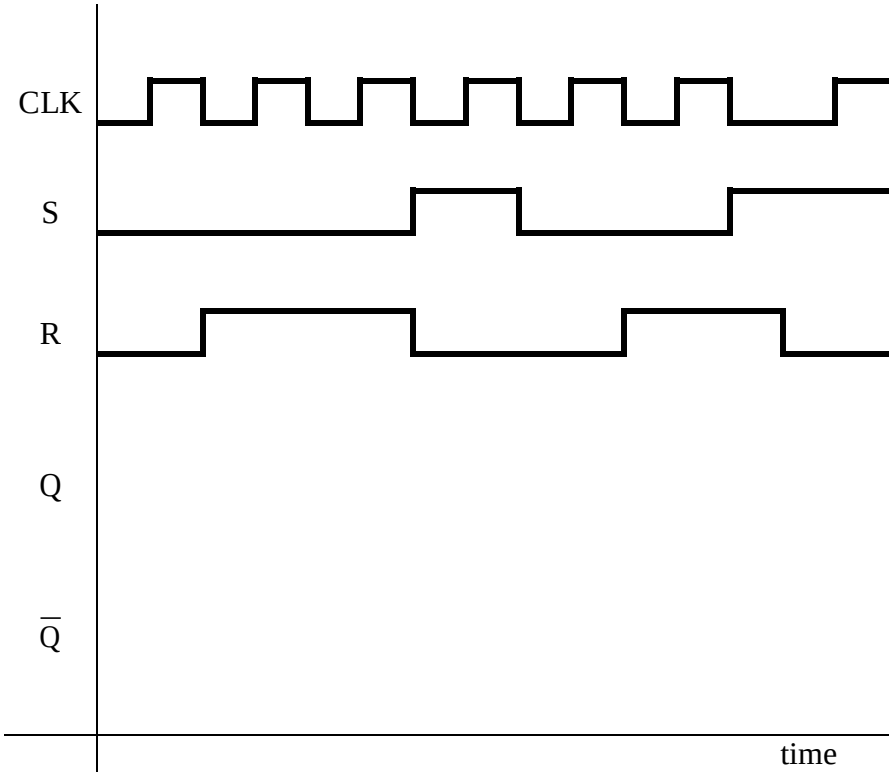
Question 4 ***(7 marks)***

a) Implement **half adder** circuit using **4:1 multiplexers** only. ***(2.5 marks)***

Solution

b) Draw the waveforms at outputs Q and $\overline{Q}$ for the following logic circuit, assume the **initial** value of Q is **logic 1**: ***(2 marks)***





c) Draw Three-bit **asynchronous** binary counter using **JK flip flops** and its timing diagram for one cycle. ***(2.5 marks)***

Solution

Question 5 ***(5 marks)***

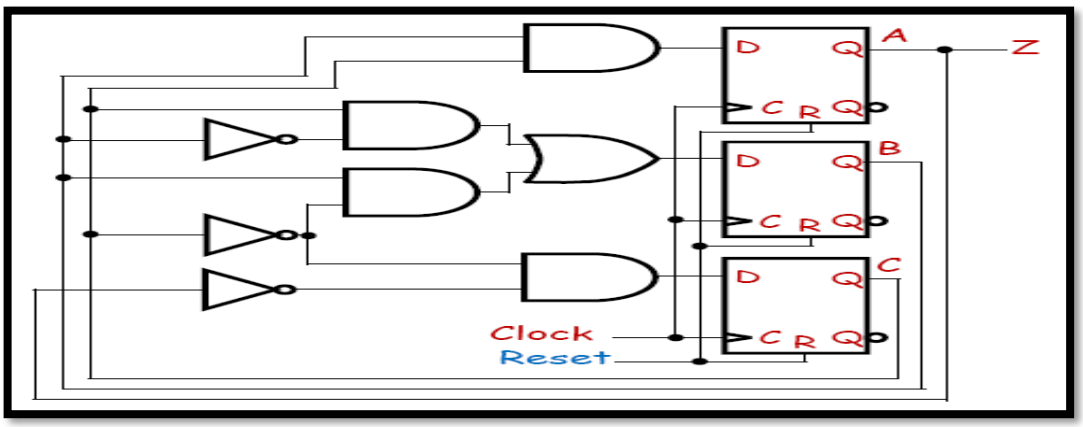
Analyze the following sequential circuit by

a) Write down the **state equations**. ***(1.5 marks)***

b) Write down the **output equations**. ***(0.5 mark)***

c) Write down the **state table** for the sequential circuit. ***(1.5 marks)***

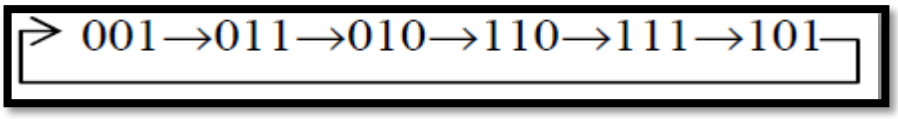
d) Draw the **state diagram** for the sequential circuit. ***(1.5 marks)***



Solution

Question 6 ***(6 marks)***

Design a **3-bit counter**, which counts in the sequence:



Use **clocked T flip-flops**

Solution

GOOD LUCK