"Design of Counters"

A sequential Circuit that goes through a prescribed Sequence of states upon the application of input pulses is Called **a counter.**

The input pulses, called **count pulses**, may be clock pulses.

In a Counter, the sequence of states may follow a binary Count or any other sequence of states.

A counter that follows the binary sequence is called **a binary counter.**

An n-bit binary counter consists of n flip-flops and can count in binary from 0 to $2^n - 1$.

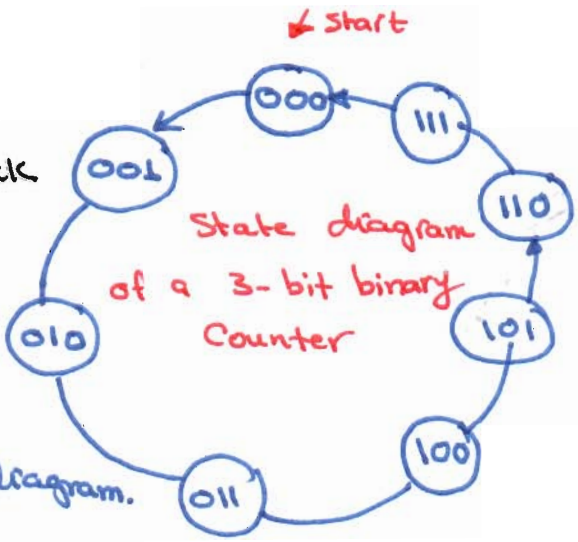
Binary Counters' Design

Example 1: Design a synchronous Counter which Counts as the following 0, 1, 2, 3, 4, 5, 6, 7 using JK flip-flops.

Design steps:

1. Construct the state diagram; which is shows the sequence of states which the counter advances when it is clocked.

* The Circuit has no inputs other than the clock pulse and no outputs other than the outputs of each flip-flop.



2. obtain the next-state table from the state diagram.

= State table =

Present State Q_2	Q_1	Q_0	Next State Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

Since there are eight states, the number of flip-flops required would be three.

3. Implement the counter design using JK flip-flops (2)

- develop the excitation table from the state table:

Output State Transition						Flip-flop Inputs					
Present state			Next state								
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	0	0	X	1	X	1	X	1

4. Transfer the JK states of the flip-flop inputs from the excitation table to Karnaugh maps.

J_2

$Q_2Q_1 \backslash Q_0$	0	1
00	0	0
01	0	1
11	X	X
10	X	X

J_1

$Q_2Q_1 \backslash Q_0$	0	1
00	0	1
01	X	X
11	X	X
10	0	1

J_0

$Q_2Q_1 \backslash Q_0$	0	1
00	1	X
01	1	X
11	1	X
10	1	X

K_2

$Q_2Q_1 \backslash Q_0$	0	1
00	X	X
01	X	X
11	0	1
10	0	0

K_0

$Q_2Q_1 \backslash Q_0$	0	1
00	X	1
01	X	1
11	X	1
10	X	1

K_1

$Q_2Q_1 \backslash Q_0$	0	1
00	X	X
01	0	1
11	0	1
10	X	X

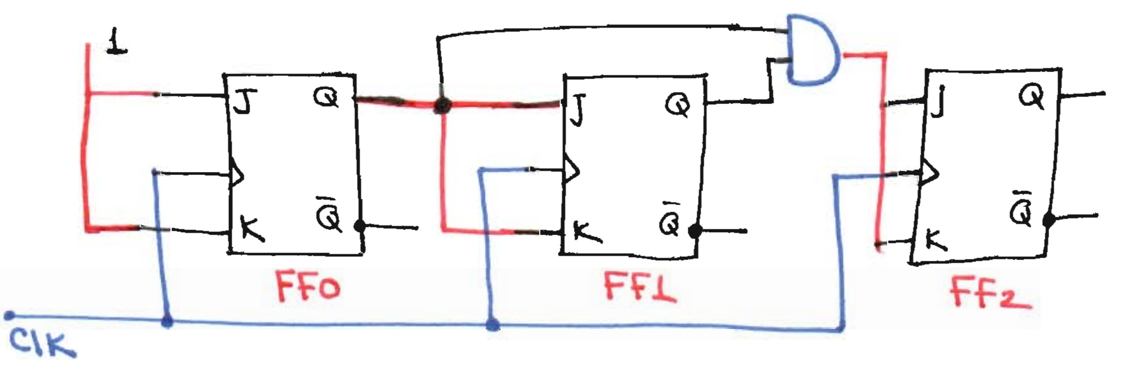
Simplified equations:

$J_0 = K_0 = 1$

$J_1 = K_1 = Q_0$

$J_2 = K_2 = Q_1 \cdot Q_0$

5. Implement the sequential Circuit (flip-flops + combinational Circuit).



logic diagram of a 3-bit binary counter

Example 2: Design a synchronous counter which counts as the following 0, 1, 2, 3, 4, 5, 6 using T flip-flops.

Design steps:

steps 1 and 2 : the same as in the previous example

3- excitation table :

Output State Transition						Flip-flop Inputs		
Present State			Next state					
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	T_2	T_1	T_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

4. Karnaugh maps :

T_2 map

Q_2Q_1 \ Q_0	0	1
00	0	0
01	0	1
11	0	1
10	0	0

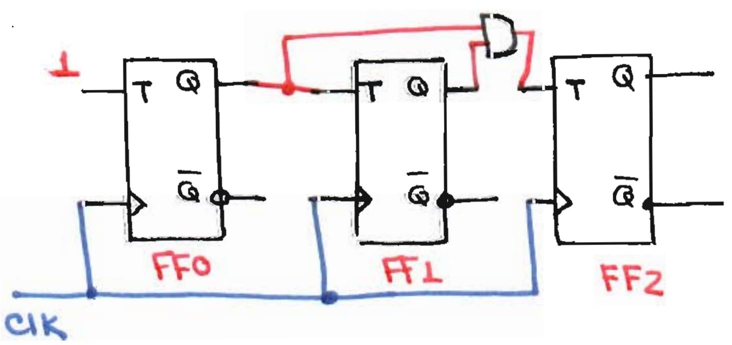
T_1 map

Q_2Q_1 \ Q_0	0	1
00	0	1
01	0	1
11	0	1
10	0	1

T_0 map

Q_2Q_1 \ Q_0	0	1
00	1	1
01	1	1
11	1	1
10	1	1

$T_0 = 1$; $T_1 = Q_0$, $T_2 = Q_1 \cdot Q_2$



Example 3: Design a synchronous counter which counts as the following 0, 1, 2, 3, 4, 5, 6, 7 using D flip-flops:

Design steps:

Steps 1 and 2: the same as in the previous example.

3- excitation table:

Present state			Next state		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

* Note:

$Q(t+1) = D$

Karnaugh map:

Q_2 \ Q_1Q_0	00	01	11	10
0			1	
1	1	1		1

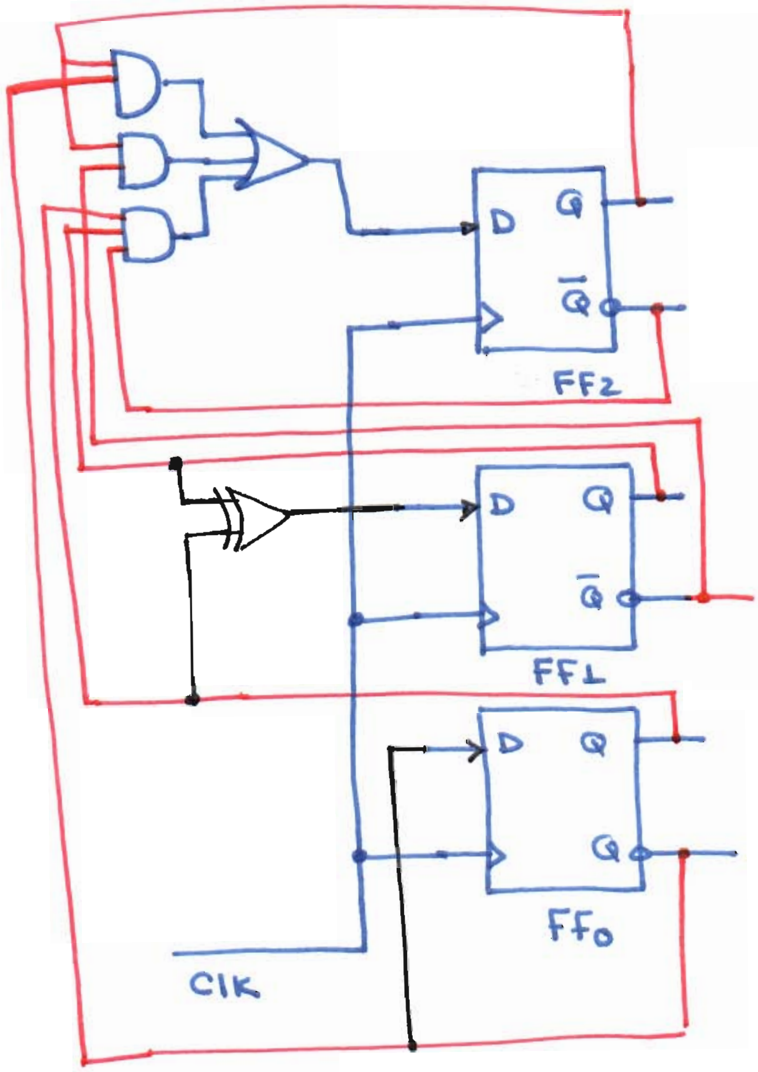
$$Q_2^{(t+1)} = Q_2 \cdot \overline{Q}_0 + Q_2\overline{Q}_1 + \overline{Q}_2 Q_1 Q_0$$

Q_2 \ Q_1Q_0	00	01	11	10
0		1		1
1		1		1

$$Q_1^{(t+1)} = \overline{Q}_1 Q_0 + Q_1 \overline{Q}_0 = Q_1 \oplus Q_0$$

Q_2 \ Q_1Q_0	00	01	11	10
0	1			1
1	1			1

$$Q_0^{(t+1)} = \overline{Q}_0$$



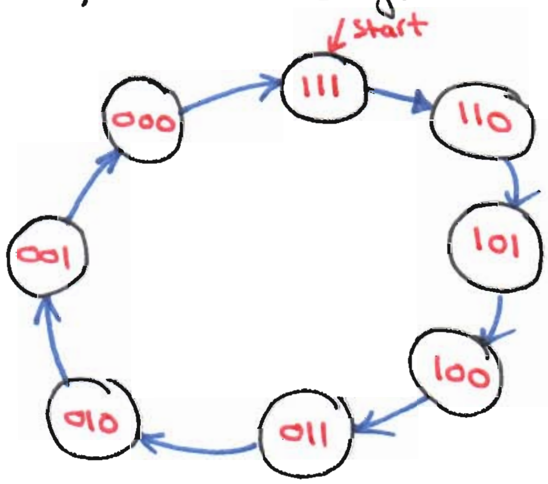
Example 4:

Design a synchronous counter which counts as the following: 7, 6, 5, 4, 3, 2, 1, 0 using JK flip-flops

- Solution:

This kind of counters is called count-down counter, in the previous examples, it is called count-up counter.

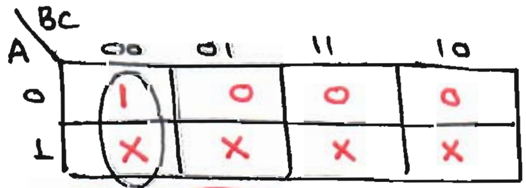
1) State diagram:



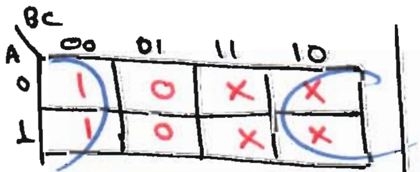
2) State table & excitation

Present state			Next state			Input equations					
A	B	C	A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
1	1	1	1	1	0	X	0	X	0	X	1
1	1	0	1	0	1	X	0	X	1	1	X
1	0	1	1	0	0	X	0	0	X	X	1
1	0	0	0	1	1	X	1	1	X	1	X
0	1	1	0	1	0	0	X	X	0	X	1
0	1	0	0	0	1	0	X	X	1	1	X
0	0	1	0	0	0	0	X	0	X	X	1
0	0	0	1	1	1	1	X	1	X	1	X

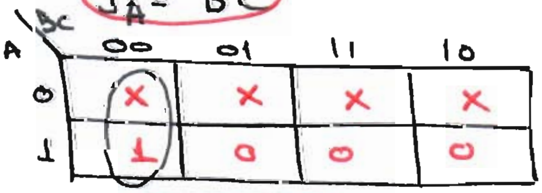
$J_C = 1$, $K_C = 1$



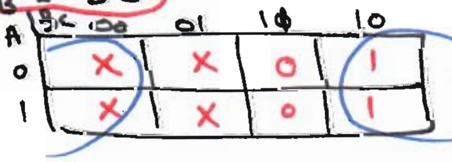
$J_A = \bar{B}\bar{C}$



$J_B = \bar{C}$



$K_B = \bar{B}\bar{C}$



$K_B = \bar{C}$