Microprocessors (0630371) Fall 2010/2011 – Lecture Notes # 3

Outline of the Lecture

> Brief History of 80x86 Family of Microprocessors.

> Registers of 80x86 Family of Microprocessors.

Brief History of 80x86 Family of Microprocessors

The principle way in which MPU & microcomputer are categorized in term of the maximum number of binary bit in the data they process that is, their word length. Processor vary in their speed, capacity of memory, register and data bus, below are a brief description of various Intel processor in Table.

Processor	Year Intro.	Transistors	Clock Rate (MHz.)	External Data Bus	Internal Data Bus	Add. Bus
4004	1971	2,250	0.108	4	8	12
8008	1972	3,500	0.200	8	8	14
8080	1974	6,000	3	8	8	16
8085	1976	6,000	6	8	8	16
8086	1978	29,000	10	16	16	20
8088	1979	29,000	10	8	16	20
80286	1982	134,000	12.5	16	16	25
80386DX	1985	275,000	33	32	32	32
80386SX	1988	275,000	33	16	32	24
Pentium C	1993	3,100,000	66 -200	64	32	32
Pentium MMX	1997	4,500,000	300	64	32	32
Pentium Pro	1995	5,500,000	200	64	32	36
Pentium II	1997	7,500,000	233-450	64	32	36
Pentium III	1999	9,500,000	550-733	64	32	36
Itanium	2001	30,000,000	800	128	64	64

Evolution of Intel's 80X86 Family Microprocessors

Different Microprocessor features descriptions

Evolution from 8080/8085 to 8086

Intel introduced 8086 microprocessor in 1978. This 16-bit microprocessor was a major improvement over the previous generation of 8080/8085 series of microprocessors.

8086	8080/8085		
1 megabyte	Memory of 64 kilobyte		
(20-bit add. bus)	(16-bit add. bus)		
16-bit Data bus	8-bit data bus		
Pipelined processor	Non-pipelined µpr		
(first single-chip µpr.)			

In a system with pipelining, the data and the address bus are busy transferring data while the CPU is processing information.

Evolution from 8086 to 8088

▶ 8086 was with 16-bit data bus internally and externally. All registers and the data bus carrying data in/out of the CPU were 16-bit. That time all the peripherals were designed around 8-bit microprocessor and It was expensive to built PCB with 16-bit data bus.

▶ So Intel introduced 8088 which was; Identical to 8086 internally, but externally 8-bit data bus instead of 16bit. IBMs decision to pick up 8088 as their choice of microprocessor in designing the IBM PC. 8088-based IBM PC was enormous success, because IBM and Microsoft made it an open system.

8088 and 8086 functionally identical but 8088 lower performance, 80186 run all 8088 and 8086 software, but have 10 new instructions. 80188 in function is identical to 80186 but lower performance. 80286 run all 8086, 80186 program, but has extra instruction, more powerful than 8086. 83086 has various operation mode, which allow it to act as 80286 chip or multiple 8086 chip, as well as a set of instruction capable of 32 bit operations such as arithmetic.

Other microprocessors: the 80286, 803386, and 80486 **80286**

- 16-bit internal and external data bus.
- 24-bit address bus
- Support three operations modes:
- *Virtual memory*: a way of access to unlimited memory by swapping data between disk storage and RAM.
- *Real mode* (faster operation with maximum of 1 Mbytes of memory)
- *Protected mode* mode is slower but can use 16 Mbytes of memory.

80386

- 32-bit internal and external data bus.
- 32-bit address bus $(2^{32} = 4 \text{ gigabyte-physical memory})$. With virtual memory 64 terabytes.
- 80386SX was later introduced with the same internal structure with 16-bit external data bus and
- 24-bit address bus. 80386SX was much cheaper.

All microprocessors discussed so far were general-purpose microprocessors and could not handle mathematical operations rapidly. For this reason, *8087*, *80287*, *80387* numeric data processing chips called *math co-processors* were used.

80486

- 32-bit internal-external data bus and 32-bit address bus.
- Built in math co-processor in a single chip.
- Introduction of *cache memory* (Static RAM with very fast access time)

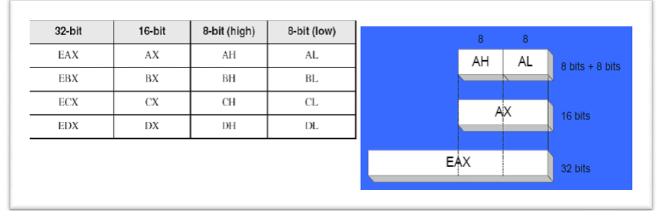
Registers of 80x86 Family of Microprocessors

	32-bit Names 10-bit Names 8-bit Names
64-bit Names /	32-bit Names 16-bit Names 8-bit Names
/	
HAX	EAX AX AH AL
FUBX	Enx BX BH BL
RCX	ECX CX CH GL
RIDX	EDX DX DH DL
RBP	EBP BP
FLS1	ESI SI
RDI	EDI DI
BSP	ESP SP
64 bits	
	- 32 bits -
	16 bits
Ra	
R9	
FI10	
B11	
H12	
R13	
B14	
R15	
	· · · · · · · · · · · · · · · · · · ·
BELAGS	
HFLAGS	EFLAGS FLAGS
1411P	EIP IP
	CS
	DS
	EB
	88
	FS
	98

The programming model of the 8086 through the Core2 microprocessor including the 64-bit extensions.

Accessing Parts of Registers.

Use 8-bit name, 16-bit name, or 32-bit name: Applies to EAX, EBX, ECX, and EDX

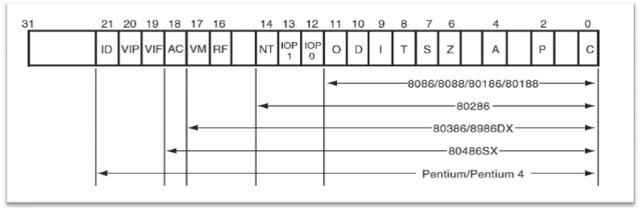


Accessing Parts of Registers

> The top portion of the programming model contains the general purpose registers: EAX, EBX, ECX, EDX, EBP, ESI, and EDI.

> R8 -R15found in the Pentium 4 and Core2 if 64-bit extensions are enabled.

> EFLAG and FLAG register



EFLAG and FLAG register

The EFLAG and FLAG register counts for the entire 8086 and Pentium microprocessor family.

> IOPL used in protected mode operation to select the privilege level for I/O devices.

NT (nested task) flag indicates the current task is nested within another task in protected mode operation.

RF (resume) used with debugging to control resumption of execution after the next instruction.

VM (virtual mode) flag bit selects virtual mode operation in a protected mode system.

AC, (alignment check) flag bit activates if a word or double word is addressed on a non-word or non-double word boundary.

VIF is a copy of the interrupt flag bit available to the Pentium 4–(virtual interrupt).

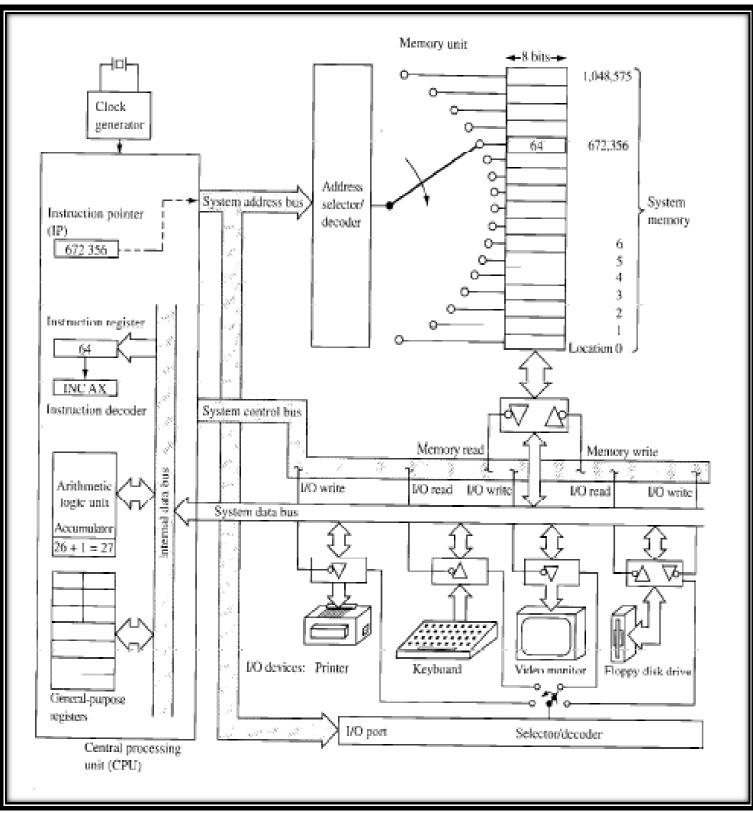
VIP (virtual) provides information about a virtual mode interrupt for (interrupt pending) Pentium. –used in multitasking environments to provide virtual interrupt flags.

ID (identification) flag indicates that the Pentium microprocessors support the CPUID instruction. –CPUID instruction provides the system with information about the Pentium microprocessor.

Registers types

1. Program visible.-registers are used during programming and are specified by the instructions.

2. Program invisible.-not addressable directly during applications programming.



Interaction between the CPU, memory and I/O Devices