Marking Scheme

Exam Paper
BSc CE

Logic Circuits (630211)

Final Exam First semester Date: 03/02/2019
Section 1

Weighting 40% of the module total

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Coordinator: Dr. Qadri Hamarsheh
Internal Examiner: Dr. Naser Halasa
Marking Scheme
Logic Circuits (630211)

The presented exam questions are organized to overcome course material through 6 questions. The all questions are compulsory requested to be answered.

Marking Assignments

**Question 1** This question is attributed with 10 marks if answered properly; the answers are the following:

1) Which of the following is not a weighted value positional numbering system:
   a) hexadecimal
   b) binary
   c) binary-coded decimal
   d) octal

2) Convert 527\textsubscript{8} to binary.
   a) 011100111
   b) 101010111
   c) 111010101
   d) 343

3) The **Gray code** of the binary number 0101 is
   a) 1111
   b) 1000
   c) 0111
   d) None of the above

4) Simplification of the Boolean expression \( AB + ABC + ABCD + ABCDE + ABCDEF \) yields which of the following results?
   a) \( AB \)
   b) \( AB + CD + EF \)
   c) \( ABCDEF \)
   d) \( A + B + C + D + E + F \)

5) Applying DeMorgan's Law to \( f = \overline{\overline{AB} + C + E + D} \) will result in:
   a) \( f = \overline{\overline{A} + \overline{B} + \overline{C} + \overline{E} + \overline{D}} \)
   b) \( f = \overline{AB} \overline{C} + E \overline{D} \)
   c) \( f = \overline{A} \overline{B} \overline{C} + (E + \overline{D}) \)
   d) \( f = \overline{A} + \overline{B} + \overline{C} + \overline{ED} \)

6) From the truth table below, determine the standard **SOP** expression.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>( A )</th>
<th>( B )</th>
<th>( C )</th>
<th>( X )</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>01</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>10</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

   a) \( X = ABC + \overline{ABC} + \overline{ABC} \)
   b) \( X = \overline{AB}C + ABC + \overline{ABC} \)
   c) \( X = ABC + \overline{ABC} + \overline{ABC} \)
   d) \( X = \overline{A} \overline{B} \overline{C} + \overline{ABC} + \overline{ABC} \)

7) The logic function implemented by the circuit below is (ground implies a logic “0”)

8) The characteristic equation of \( S-R \) latch is

   a) \( Q(n + 1) = S'R + Q(n)R \)
   b) \( Q(n + 1) = (S + Q(n))R \)
   c) \( Q(n + 1) = S'R + Q(n)R \)
   d) \( Q(n + 1) = S'R + Q'(n)R \)
9) The figure shown below is ------

![Diagram]

a) A T flip flop  b) An S-R latch  
c) A JK flip flop  d) A D flip flop

10) A ripple counter is a(n) --------- device  
a) asynchronous  b) Combinational  
c) synchronous  d) None of them

Question 2 This question is attributed with 6 marks if answered properly; the answers are the following:

a) Prove the identity of the following Boolean equation, using algebraic manipulation:  

\[ \overline{AB} + \overline{BC} + AB + \overline{BC} = 1 \]  

Solution:

\[ \begin{align*}
\overline{A}B + \overline{B}C + AB + \overline{B}C &= 1 \\
&= (\overline{A} B + \overline{B}) + (\overline{C} + B) (\overline{C}) \\
&= B(A + \overline{A}) + \overline{B}(C + \overline{C}) \\
&= B + \overline{B} \\
&= 1
\end{align*} \]

b) Draw 4-bit asynchronous binary counter using JK flip flops and its timing diagram. (4 marks)
**Question 3** This question is attributed with 4 marks if answered properly; the answers are the following: Implement full adder circuit using 4:1 multiplexers.

<table>
<thead>
<tr>
<th>x</th>
<th>y</th>
<th>Cin</th>
<th>S</th>
<th>Cout</th>
<th>S</th>
<th>Cout</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
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<td>1</td>
<td>z</td>
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</tbody>
</table>

**Solution**

**Question 4** This question is attributed with 7 marks if answered properly; the answers are the following:

a) Derive the Boolean equations for D and $B_{out}$. (3 marks)

$D = P\overline{Q}B_{in} + P\overline{Q}B_{in} + PQ\overline{B}_{in} + PQB_{in} + PQB_{in}$

$b) Implement D and $B_{out}$ logic circuits. (2 marks)

**c) Design the 1-bit full subtractor using 3x8 decoder. (2 marks)**

**Question 5** This question is attributed with 6 marks if answered properly; the answers are the following:
Solution

The flip flop input equations are

\[
D_1 = xq_1 + xq_2 \\
D_2 = xq'_1 q'_2 \\
z = xq_1
\]

The output equations are

D flip flops \( q^* = D \) Thus

\[
q^*_1 = xq_1 + xq_2 \\
q^*_2 = xq'_1 q'_2
\]

State table

<table>
<thead>
<tr>
<th>( q )</th>
<th>( x = 0 )</th>
<th>( x = 1 )</th>
<th>( z )</th>
<th>( x = 0 )</th>
<th>( x = 1 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>0 0</td>
<td>0 1</td>
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<tr>
<td>0 1</td>
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<tr>
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<td></td>
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<td>0 0</td>
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<td>0</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

State diagram

Question 6 This question is attributed with 7 marks if answered properly; the answers are the following:
The **next state** table for this state diagram (1.5 marks)

<table>
<thead>
<tr>
<th>Input</th>
<th>Current State</th>
<th>Next State</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>Q1</td>
<td>Q0</td>
<td>Q1</td>
</tr>
<tr>
<td>0</td>
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</tbody>
</table>

The **excitation equations** if **J-K flip flops** are used to implement this state diagram (use the Karnaugh map in your solution).

**J-K flip flop transition table:** (2 marks)

<table>
<thead>
<tr>
<th>Qcurrent</th>
<th>Qnext</th>
<th>J</th>
<th>K</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
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<td>0</td>
<td>x</td>
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<tr>
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</table>

**Karnaugh map** (2 marks)

The logic circuit using **J-K flip flops** (1.5 marks)