Philadelphia University
Faculty of Engineering

Marking Scheme

Exam Paper

BSc CE

Logic Circuits (630211)

Final Exam	First semester	Date: 03/02/2019

Section 1

Weighting 40% of the module total

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Marking Scheme

Logic Circuits (630211)

The presented exam questions are organized to overcome course material through 6 questions.
The *all questions* are compulsory requested to be answered.

Marking Assignments

Question 1 This question is attributed with ***10 marks*** if answered properly; the answers are the following:

1) Which of the following is **not a weighted** value positional numbering system?

a)	**hexadecimal**	**b)**	**binary**
c)	**binary-coded decimal**	**d)**	**octal**

2) Convert 527_8 to binary.

a)	**011100111**	**b)**	**101010111**
c)	**111010101**	**d)**	**343**

3) The **Gray code** of the binary number **0101** is

a)	**1111**	**b)**	**1000**
c)	**0111**	**d)**	**None of the above**

4) Simplification of the Boolean expression $AB + ABC + ABCD + ABCDE + ABCDEF$ yields which of the following results?

a)	**AB**	**b)**	**AB + CD + EF**
c)	$ABCDEF$	**d)**	**A + B + C + D + E + F**

5) Applying **DeMorgan's Law** to $f = \overline{\overline{AB} + \overline{C}\left(E + \overline{D}\right)}$ will result in:

a)	$f = \overline{A} + \overline{B} + \overline{C} + \overline{E} + D$	**b)**	$f = \overline{A}\,\overline{B}\,\overline{C} + E\overline{D}$
c)	$f = \overline{A}\,\overline{B}\,\overline{C} + (E + \overline{D})$	**d)**	$f = \overline{A} + \overline{B} + \overline{C} + E\overline{D}$

6) From the truth table below, determine the standard **SOP** expression.

Inputs			Output
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

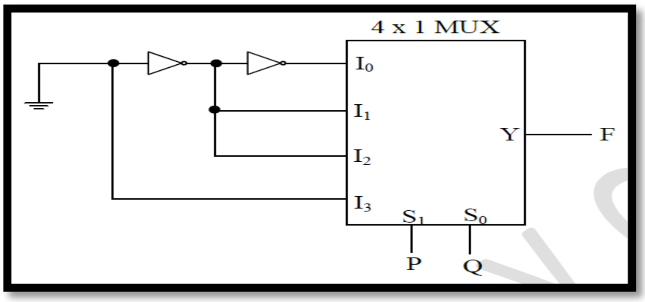
a) $X = \overline{A}\,\overline{B}C + \overline{A}BC + AB\overline{C}$

b) $X = \overline{A}\,\overline{B}\,\overline{C} + ABC + A\overline{B}C$

c) $X = ABC + ABC + ABC$

d) $X = A\overline{B}C + \overline{A}BC + AB\overline{C}$

7) The logic function implemented by the circuit below is (ground implies a logic "0")

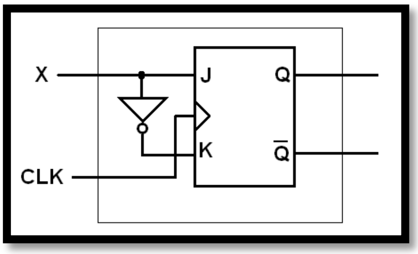


a)	$F = AND\,(P, Q)$	**b)**	$F = OR\,(P, Q)$
c)	$F = XOR\,(P, Q)$	**d)**	$F = XNOR\,(P, Q)$

8) The characteristic equation of **S-R** latch is

a)	$Q(n+1) = S'R + Q(n)R$	**b)**	$Q(n+1) = (S + Q(n))R'$
c)	$Q(n+1) = SR + Q(n)R$	**d)**	$Q(n+1) = S'R + Q'(n)R$

9) The figure shown below is -------



a) **A T flip flop**

b) **An S-R latch**

c) **A JK flip flop**

d) **A D flip flop**

10) A **ripple counter** is a(n) ---------- device

a) **asynchronous**

b) **Combinational**

c) **synchronous**

d) **None of them**

<u>Question 2</u> This question is attributed with ***6 marks*** if answered properly; the answers are the following:

a) Prove the identity of the following Boolean equation, using **algebraic manipulation**:

(2 marks)

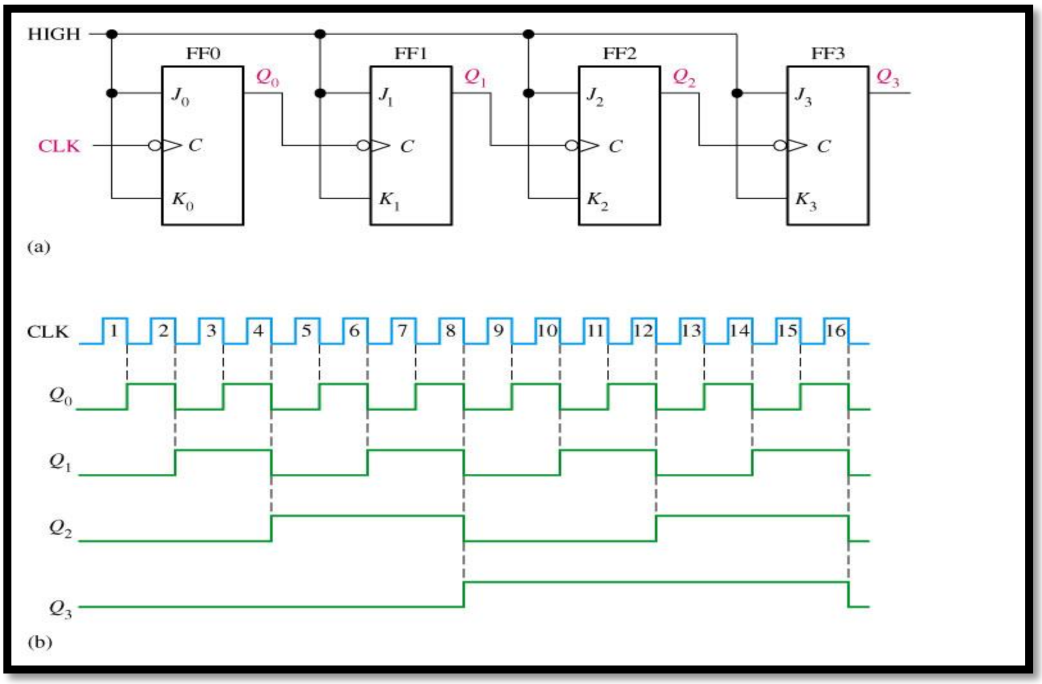
$$\overline{A}B + \overline{B}\overline{C} + AB + \overline{B}C = 1$$

Solution

$$\overline{A}B + \overline{B}\,\overline{C} + AB + \overline{B}C = 1$$
$$= (\overline{A}B + AB) + (\overline{B}\,\overline{C} + \overline{B}C)$$
$$= B(A + \overline{A}) + \overline{B}(C + \overline{C})$$
$$= B + \overline{B}$$
$$= 1$$

b) Draw **4-bit asynchronous** binary counter using **JK** flip flops and its timing diagram. ***(4 marks)***

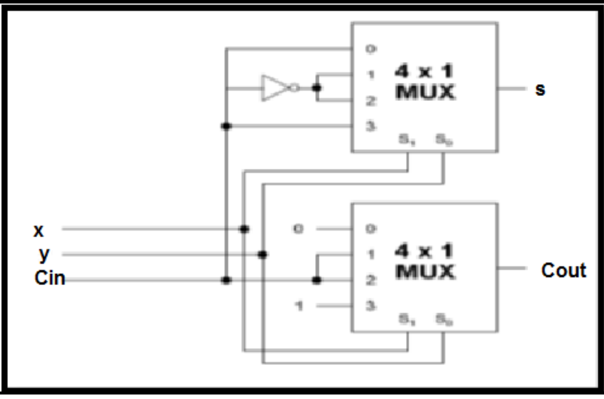
Solution



Question 3 This question is attributed with ***4 marks*** if answered properly; the answers are the following:
Implement **full adder** circuit using **4:1 multiplexers**.

Solution

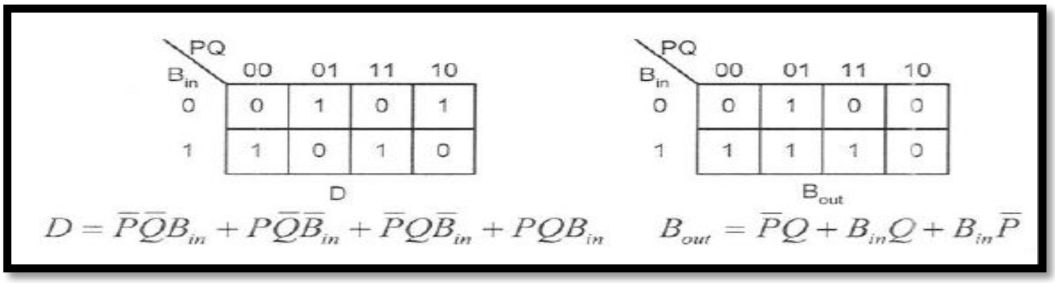
x	y	Cin	S	Cout	S	Cout
0	0	0	I_0=z	I_0=0	0	0
0	0	1			1	0
0	1	0	I_1=z'	I_1=z	1	0
0	1	1			0	1
1	0	0	I_2=z'	I_2=z	1	0
1	0	1			0	1
1	1	0	I_3=z	I_3=1	0	1
1	1	1			1	1



Question 4 This question is attributed with ***7 marks*** if answered properly; the answers are the following:

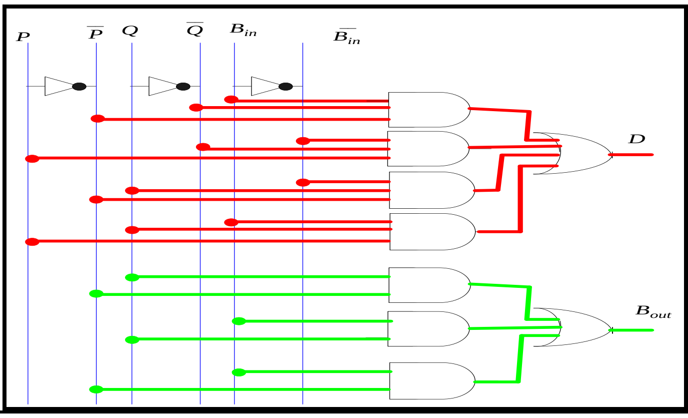
a) Derive the Boolean equations for D and B_{out}. ***(3 marks)***

Solution



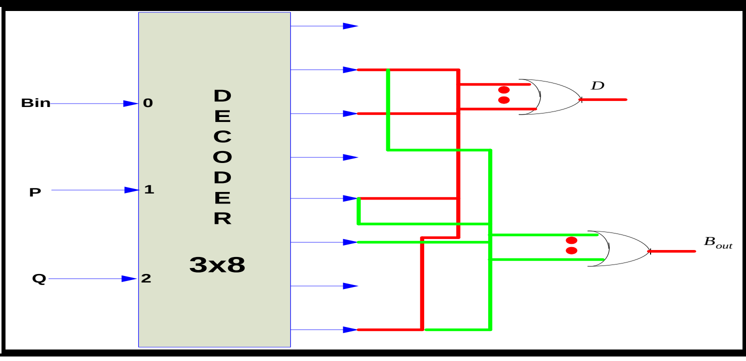
b) Implement D and B_{out} logic circuits. ***(2 marks)***

Solution



c) Design the 1-bit full subtractor using 3x8 decoder. ***(2 marks)***

Solution



Question 5 This question is attributed with ***6 marks*** if answered properly; the answers are the following:

Solution

The flip flop input equations are

$$D_1 = xq_1 + xq_2$$
$$D_2 = xq_1'q_2'$$
$$z = xq_1$$

The output equations are

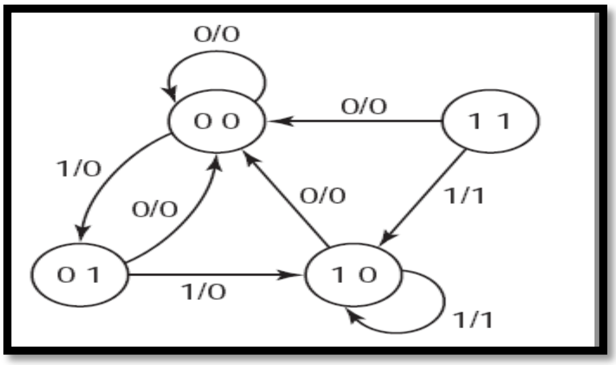
***D* flip flops** $q^\star = D$ **Thus**

$$q_1^\star = xq_1 + xq_2$$
$$q_2^\star = xq_1'q_2'$$

State table

q	$q^\star$ $x = 0$	$x = 1$	z $x = 0$	$x = 1$
0 0	0 0	0 1	0	0
0 1	0 0	1 0	0	0
1 0	0 0	1 0	0	1
1 1	0 0	1 0	0	1

State diagram



Question 6 This question is attributed with ***7 marks*** if answered properly; the answers are the following:

The **next state** table for this state diagram *(1.5 marks)*

Input	Current State		Next State		Output
X	Q1	Q0	Q1	Q0	Y
0	0	0	1	1	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	0	0	1
1	1	0	1	1	0
1	1	1	0	1	0

The **excitation equations** if **J-K flip flops** are used to implement this state diagram (use the Karnaugh map in your solution).
J-K flip flop transition table: *(2 marks)*

$Q_{current}$	Q_{next}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Input	Current State		Next State		Output	flip flop inputs (excitation)			
X	Q1	Q0	Q1	Q0	Y	J1	K1	J0	K0
0	0	0	1	1	0	1	x	1	x
0	0	1	0	0	1	0	x	x	1
0	1	0	0	1	0	x	1	1	x
0	1	1	1	0	0	x	0	x	1
1	0	0	1	0	0	1	x	0	x
1	0	1	0	0	1	0	x	x	1
1	1	0	1	1	0	x	0	1	x
1	1	1	0	1	0	x	1	x	0

Karnaugh map *(2 marks)*

J1

XQ1 \ Q0	0	1
00	1	0
01	x	x
11	x	x
10	1	0

$J1 = \overline{Q0}$

K1

XQ1 \ Q0	0	1
00	x	x
01	1	0
11	x	x
10	0	1

$K1 = \overline{X}\,\overline{Q0} + XQ0$

J0

XQ1 \ Q0	0	1
00	1	x
01	1	x
11	1	x
10	x	0

$J0 = \overline{X} + Q1$

K0

XQ1 \ Q0	0	1
00	x	1
01	x	1
11	x	0
10	x	1

$K0 = \overline{X} + \overline{Q1}$

Y

XQ1 \ Q0	0	1
00	0	1
01	0	0
11	0	0
10	0	1

$Y = \overline{Q1}Q0$

The logic circuit using **J-K flip flops** *(1.5 marks)*