Philadelphia University
Faculty of Engineering

Marking Scheme

Exam Paper

BSc CE

Logic Circuits (630211)

Final Exam | Second semester | Date: 02/06/2019

Section 1

Weighting 40% of the module total

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Marking Scheme

Logic Circuits (630211)

The presented exam questions are organized to overcome course material through 6 questions.
The *all questions* are compulsory requested to be answered.

Marking Assignments

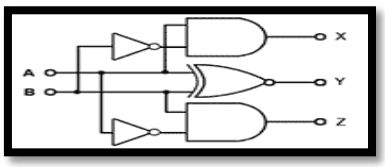
Question 1 This question is attributed with ***10 marks*** if answered properly; the answers are the following:

1) The binary number **11101011000111010** can be written in hexadecimal as _____.

a) $\mathbf{DD63A_{16}}$ **b)** $\mathbf{1D63A_{16}}$

c) $\mathbf{1D631_{16}}$ **d)** $\mathbf{1D33A_{16}}$

2) Refer to the following figure. If **A = 0** and **B = 1**, what will be the logic states at **X, Y** and **Z**?



a) **X=1, Y=1, Z=0** **b)** **X=1, Y=0, Z=0**

c) **X=0, Y=0, Z=1** **d)** **X=0, Y=1, Z=0**

3) The **simplification** of the Boolean expression $(\overline{A}B\overline{C}) + (\overline{A\overline{B}C})$ is

a) **0** **b)** **1**

c) **A** **d)** **BC**

4) The **equivalent canonical (standard) form** for the following logical expression

$\mathbf{F = AB + C}$ is

a) $\mathbf{F = ABC + \overline{A}BC + A\overline{B}C + \overline{A}\overline{B}C}$

b) $\mathbf{F = ABC + A\overline{B}C + \overline{A}\overline{B}C + AB\overline{C}}$

c) $\mathbf{F = ABC + \overline{A}BC + A\overline{B}C + \overline{A}\overline{B}C + AB\overline{C}}$

d) **None of the above**

5) The function $\mathbf{F(A,B,C)} = \sum(\mathbf{1,2,3,5,7})$ is equivalent to

a) $\overline{C} + \overline{A}B$ **b)** $C + AB$

c) $C + \overline{A}B$ **d)** $C + A\overline{B}$

6) Which of the following circuits come under the class of combinational logic circuits?

1. Full adder **2.** Full subtracter

3. Half adder **4.** J-K flip

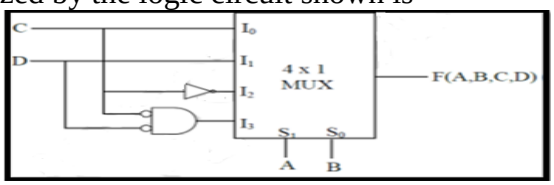
5. Counter

Select the correct answer from the codes given below:

a) **1 only** **b)** **3 and 4**

c) **4 and 5** **d)** **1, 2, and 3**

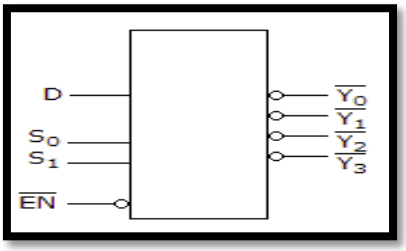
7) The Boolean function realized by the logic circuit shown is



a) $\mathbf{F = \Sigma m\,(0,1,3,5,9,10.14)}$ **b)** $\mathbf{F = \Sigma m\,(2,3,5,7,8,12.13)}$

c) $\mathbf{F = \Sigma m\,(1,2,4,5,11,14.15)}$ **d)** $\mathbf{F = \Sigma m\,(2,3,5,7,8,9.12)}$

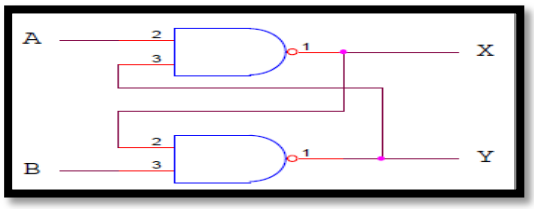
8) The circuit shown here is most likely a _____.



a) **Adder** **b)** **Multiplexer**

c) **Demultiplexer** **d)** **Parity generator**

9) If the input combination **A=0, B=1** is applied to this circuit, the (steady state) output will be:



a) **X=0, Y=0** **b)** **X=0, Y=1**
c) **X=1, Y=0** **d)** **X=1, Y=1**

10) The characteristic equation for the **T**-Flip Flop is:

a) $Q(t+1) = T.\overline{Q} + \overline{T}.Q$ **b)** $Q(t+1) = \overline{T}.\overline{Q} + T.Q$

Question 2 This question is attributed with ***6 marks*** if answered properly; the answers are the following:

a) ***(1.5 marks)***

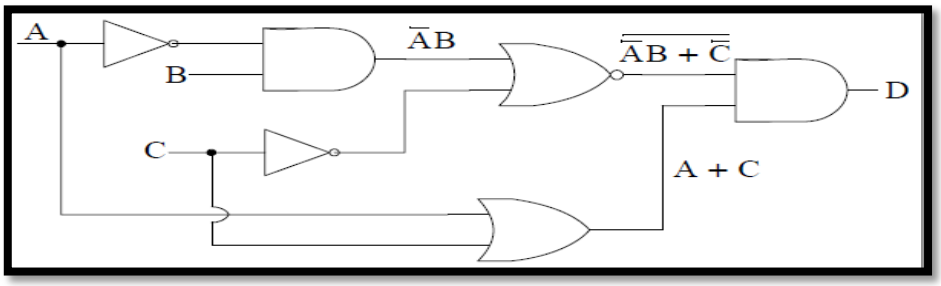
Solution

Three weighted Binary codes **codes are:**

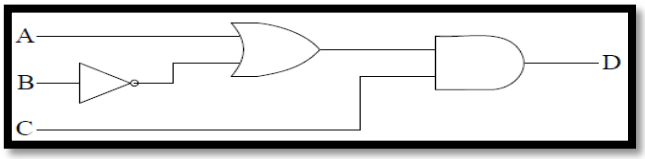
1. **BCD (8421)**
2. **6311**
3. **2421**
4. **642-3**
5. **84-2-1**

b) ***(2.5 marks)***

Solution



$$D = (\overline{\overline{A}B + \overline{C}})(A + C) = (\overline{\overline{A}}\overline{BC})(A + C) = [(A + \overline{B})C](A + C)$$
$$= (A + \overline{B})(AC + CC) = (A + \overline{B})(AC + C) = AAC + AC + A\overline{B}C + \overline{B}C$$
$$= AC + AC + \overline{B}C(A + 1) = AC + \overline{B}C(1) = AC + \overline{B}C$$
$$= (A + \overline{B})C$$



c) ***(2 marks)***

Solution

$$D = A(B + \overline{B}) + (A + \overline{A})\overline{B}C = AB + A\overline{B} + A\overline{B}C + \overline{A}\overline{B}C$$
$$D = AB(C + \overline{C}) + A\overline{B}(C + \overline{C}) + A\overline{B}C + \overline{A}\overline{B}C$$
$$= ABC + AB\overline{C} + A\overline{B}C + A\overline{B}\overline{C} + A\overline{B}C + \overline{A}\overline{B}C$$
$$D = \overline{A}\overline{B}C + A\overline{B}\overline{C} + A\overline{B}C + AB\overline{C} + ABC$$
$$= m_1 + m_4 + m_5 + m_6 + m_7 = \Sigma(1, 4, 5, 6, 7)$$

Question 3 This question is attributed with ***7 marks*** if answered properly; the answers are the following:

a) ***(4 marks)***

Solution

Inputs			Outputs	
X	Y	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth table for the full adder

$$\left.\begin{array}{l} S = C_{in} \oplus (X \oplus Y) \\ C_{out} = C_{in} \cdot (X \oplus Y) + XY \end{array}\right\}$$

Proof:

The sum:

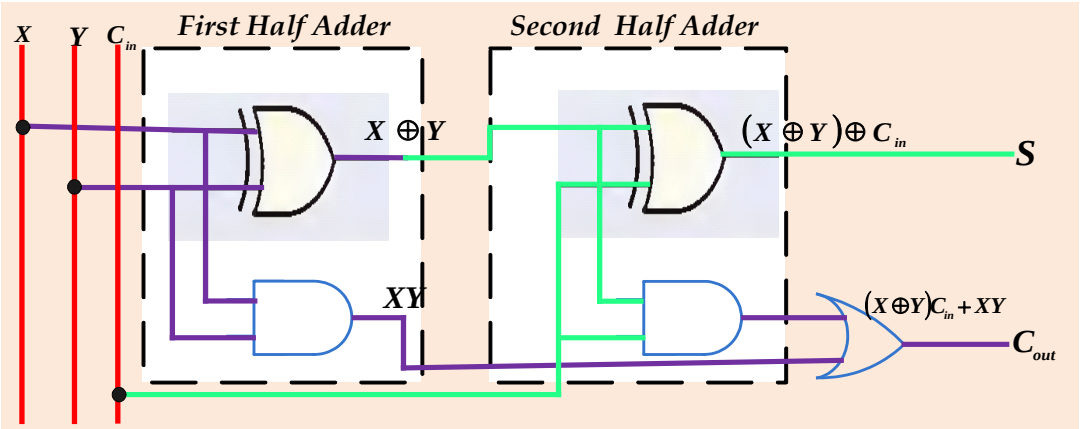
$$\begin{aligned} S &= \bar{X}\bar{Y}C_{in} + \bar{X}Y\overline{C_{in}} + X\bar{Y}\,\overline{C_{in}} + XYC_{in} \\ &= \overline{C_{in}}(\bar{X}Y + X\bar{Y}) + C_{in}(\bar{X}\bar{Y} + XY) \\ &= \overline{C_{in}}(\bar{X}Y + X\bar{Y}) + C_{in}\overline{(\bar{X}Y + X\bar{Y})} \end{aligned}$$

$$S = C_{in} \oplus (X \oplus Y)$$

The carry output:

$$\begin{aligned} C_{out} &= \bar{X}YC_{in} + X\bar{Y}C_{in} + XYC_{in} + XY\,\overline{C_{in}} \\ &= C_{in}(\bar{X}Y + X\bar{Y}) + XY(C_{in} + \overline{C_{in}}) \end{aligned}$$

$$C_{out} = C_{in} \cdot (X \oplus Y) + XY$$



Implementation of Full Adder with two Half Adders and an OR gate

b) ***(3 marks)***

Solution

CHARACTERISTIC EQUATION	EXCITATION TABLE
$Q_{(next)} = S + R'Q$ $SR = 0$	Q | Q(next) | S | R 0 | 0 | 0 | X 0 | 1 | 1 | 0 1 | 0 | 0 | 1 1 | 1 | X | 0
$Q_{(next)} = JQ' + K'Q$	Q | Q(next) | J | K 0 | 0 | 0 | X 0 | 1 | 1 | X 1 | 0 | X | 1 1 | 1 | X | 0

Question 4 This question is attributed with ***7 marks*** if answered properly; the answers are the following:

a) ***(3 marks)***

Solution

$F1 = \overline{(X + Z)} + XYZ = X'Z' + XYZ = X'Z'(Y + Y') + XYZ = X'Y'Z' + X'YZ' + XYZ$

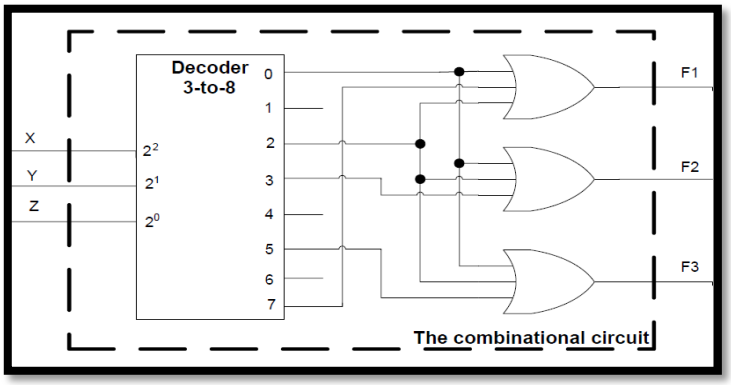
$= m0 + m2 + m7$

$F2 = \overline{(X + Z)} + X'YZ = X'Z' + X'YZ = X'Z'(Y + Y') + X'YZ = X'Y'Z' + X'YZ' + X'YZ$

$= m0 + m2 + m3$

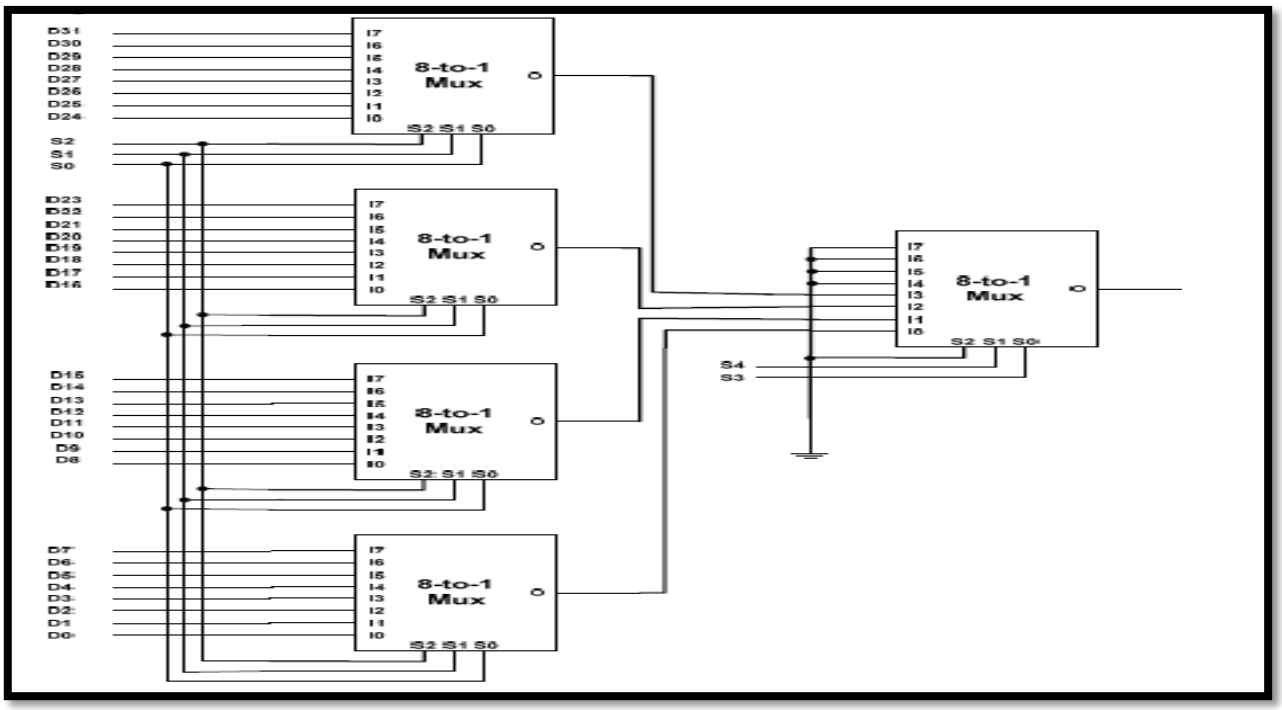
$F3 = XY'Z + \overline{(X + Z)} = XY'Z + X'Z' = XY'Z + X'Z'(Y + Y') = XY'Z + X'Y'Z' + X'YZ'$

$= m5 + m0 + m2$



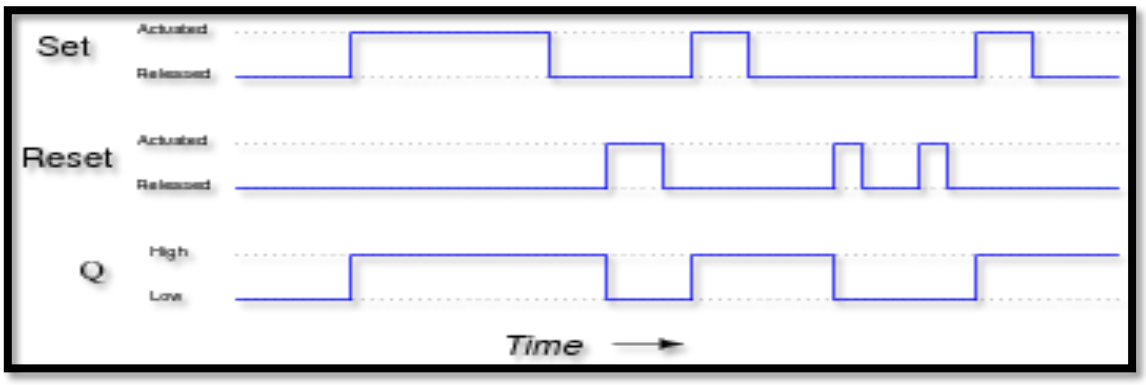
b) ***(2 marks)***

Solution



c) ***(2 marks)***

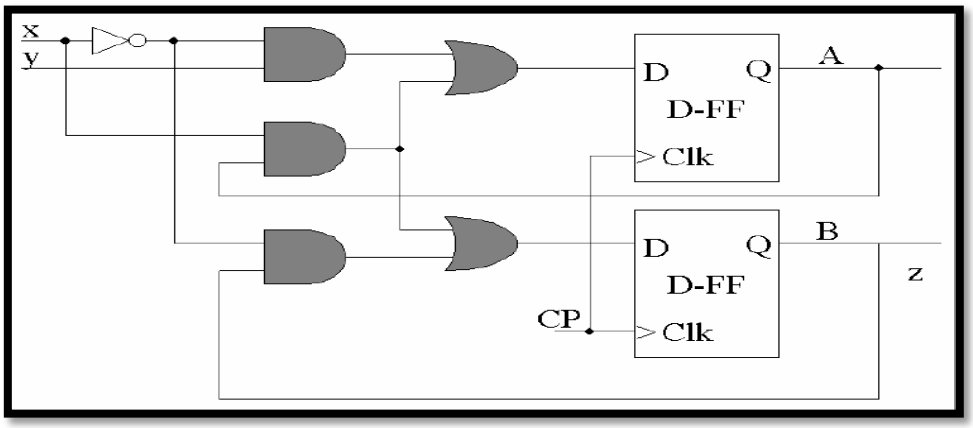
Solution



Question 5 This question is attributed with ***5 marks*** if answered properly; the answers are the following:

Solution

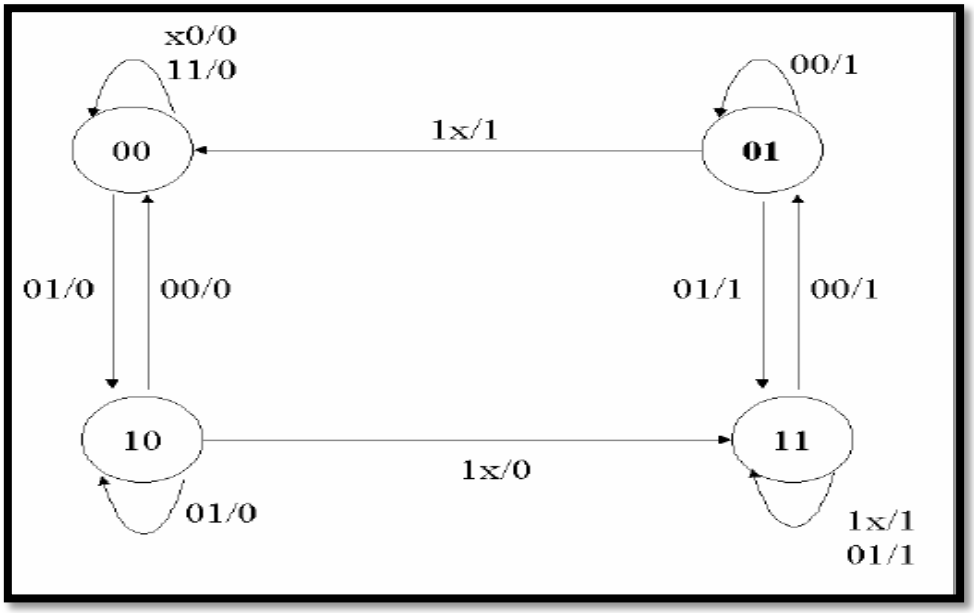
a) ***(1.5 marks)***



b) ***(2 marks)***

Present State		Inputs		Next State		Output
A	B	x	y	A	B	z
0	0	0	0	0	0	0
0	0	0	1	1	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	1	1
0	1	0	1	1	1	1
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	0	0	0
1	0	0	1	1	0	0
1	0	1	0	1	1	0
1	0	1	1	1	1	0
1	1	0	0	0	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

c) ***(1.5 marks)***



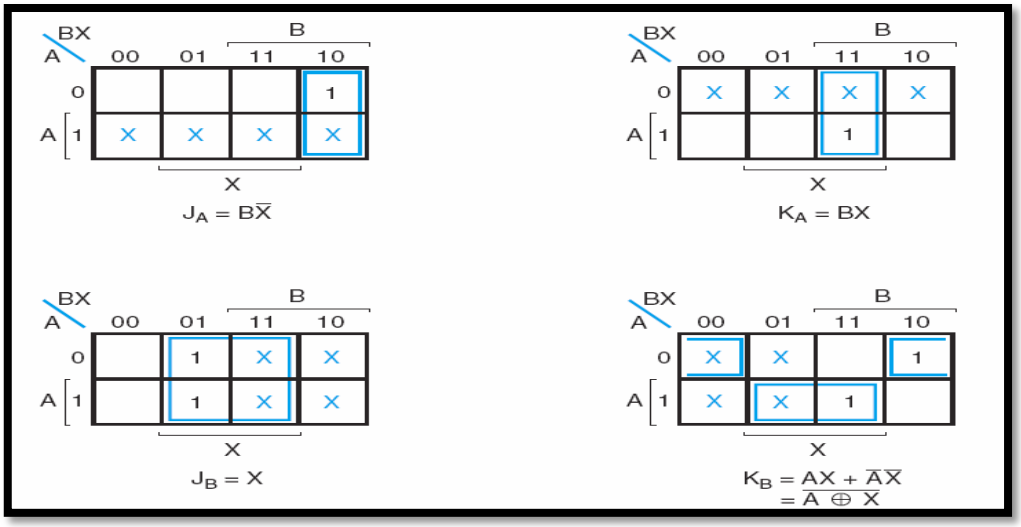
Question 6 This question is attributed with ***5 marks*** if answered properly; the answers are the following:

Solution

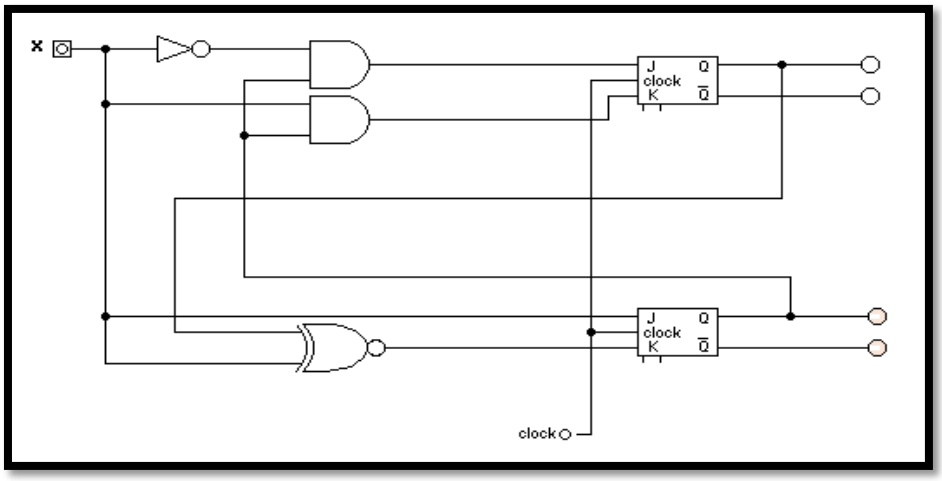
Present State		Input	Next State		Flip-Flop Inputs			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	1	0	1	X	X	1
0	1	1	0	1	0	X	X	0
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1

Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(2 marks)



(2 marks)



(1 mark)