Philadelphia University
Faculty of Engineering

Marking Scheme

Exam Paper

BSc CE

Logic Circuits (630211)

Final Exam | First semester | Date: 28/01/2020

Section 1

Weighting 40% of the module total

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Marking Scheme
Logic Circuits (630211)

The presented exam questions are organized to overcome course material through 6 questions.
The *all questions* are compulsory requested to be answered.

Marking Assignments

Question 1 This question is attributed with ***10 marks*** if answered properly; the answers are the following:
Identify the choice that best completes the statement or answers the question.

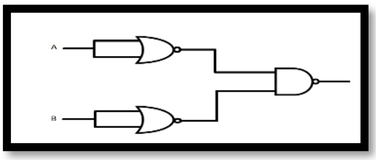
1) The **binary** number **101110101111010** can be written in **octal** as ________.

a)	**51562_8**	**b)**	**56577_8**
c)	**56572_8**	**d)**	**65627_8**

2) The **excess-3** code of decimal number **26** is:

a)	**01001101**	**b)**	**01001001**
c)	**10001001**	**d)**	**01011001**

3) In the circuit shown below, which logic function does this circuit generate?



a)	**OR**	**b)**	**AND**
c)	**NOR**	**d)**	**NAND**

4) The **dual** of the Boolean function $x + yz$ is:

a)	$\bar{x}(\bar{y} + \bar{z})$	**b)**	$x(y + z)$
c)	$x + yz$	**d)**	$\bar{x} + \bar{y}\bar{z}$

5) Applying **DeMorgan's theorem to** the expression $\overline{\overline{(X+Y)} + \overline{Z}}$, we get ________

a)	$(X+Y)Z$	**b)**	$(\overline{X}+\overline{Y})\overline{Z}$
c)	$(\overline{X}+\overline{Y})Z$	**d)**	$(X+Y)\overline{\overline{Z}}$

6) The K-map for a Boolean function is shown in the figure. The number of **essential prime implicants** for this function is

CD \ AB	00	01	11	10
00	1	1	0	1
01	0	0	0	1
11	1	0	0	0
10	1	0	0	1

a)	**4**	**b)**	**5**
c)	**6**	**d)**	**8**

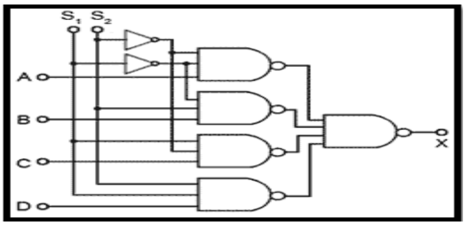
7) **Any** combinational circuit can be built using

1. *NAND gates.*
2. *NOR gates.*
3. *EX-OR gates.*
4. *Multiplexers.*

Which of these are correct?

a)	**1, 2 and 3**	**b)**	**1, 3 and 4**
c)	**2, 3 and 4**	**d)**	**1,2 and 4**

8) Refer to the following figure, If **S_1=1** and **S_2= 0** what will be the logic state at the output **X**?



a)	**X = A**	**b)**	**X = B**
c)	**X = C**	**d)**	**X = D**

9) **PRESET** and **CLEAR** inputs are normally **synchronous**.

a)	**True**	**b)**	**False**

10) When designing the circuit with the state table shown below using **JK** flip flops, then **J_A**=..., **K_A**=....

Present State A	Present State B	Input X	Next State A	Next State B	JA	KA
0	0	0	0	0		
0	0	1	0	1		
0	1	0	1	0		
0	1	1	0	1		
1	0	0	1	0		
1	0	1	1	1		
1	1	0	1	1		
1	1	1	0	0		

a) $J_A = B'.x', K_A = A'$ **b)** $J_A = B.x , K_A = A$

c) $J_A = B X , K_A = A'$ **d)** $J_A = B.x' , K_A = B.x$

Question 2 This question is attributed with ***6 marks*** if answered properly; the answers are the following:

a) ***(2 marks)***

Solution

$$= (a.b.(c+\bar{b}+\bar{d})+\bar{a}+\bar{b}).c.d \quad \text{(De Morgan)}$$
$$= (a.b.c+a.b.\bar{b}+a.b.\bar{d}+\bar{a}+\bar{b}).c.d \quad \text{(distribute)}$$
$$= (a.b.c+a.b.\bar{d}+\bar{a}+\bar{b}).c.d \quad (a.b.\bar{b}=0)$$
$$= a.b.c.d+a.b.\bar{d}.c.d+\bar{a}.c.d+\bar{b}.c.d \quad \text{(distribute)}$$
$$= a.b.c.d+\bar{a}.c.d+\bar{b}.c.d \quad (a.b.\bar{d}.c.d=0)$$
$$= (a.b+\bar{a}+\bar{b}).c.d \quad \text{(distribute)}$$
$$= (a.b+\overline{a.b}).c.d \quad \text{(DeMorgan)}$$
$$= c.d \quad (a.b+\overline{a.b}=1)$$

b) ***(4 marks)***

Solution

Function	Minterm list	Maxterm list
F	$\sum XYZ\,(3;\ 5;\ 6;\ 7)$	$\prod XYZ\,(0;\ 1;\ 2;\ 4)$
G	$\sum XYZ\,(1;\ 2;\ 4;\ 7)$	$\prod XYZ\,(0;\ 3;\ 5;\ 6)$

Question 3 This question is attributed with ***6 marks*** if answered properly; the answers are the following:

Solution

B_1B_0 \ B_3B_2	00	01	11	10
00	m0 0	m4 0	m12 0	m8 0
01	m1 1	m5 1	m13 1	m9 1
11	m3 0	m7 0	m15 0	m11 0
10	m2 1	m6 1	m14 1	m10 1

$G_0 = B_0\overline{B_1} + \overline{B_0}B_1 = B_0 \oplus B_1$

B_1B_0 \ B_3B_2	00	01	11	10
00	m0 0	m4 1	m12 1	m8 0
01	m1 0	m5 1	m13 1	m9 0
11	m3 1	m7 0	m15 0	m11 1
10	m2 1	m6 0	m14 0	m10 1

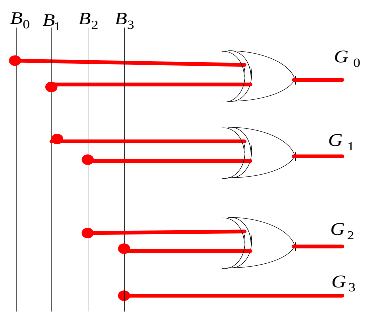
$G_1 = B_1\overline{B_2} + \overline{B_1}B_2 = B_1 \oplus B_2$

B_1B_0 \ B_3B_2	00	01	11	10
00	m0 0	m4 1	m12 0	m8 1
01	m1 0	m5 1	m13 0	m9 1
11	m3 0	m7 1	m15 0	m11 1
10	m2 0	m6 1	m14 0	m10 1

$G_2 = B_2\overline{B_3} + \overline{B_2}B_3 = B_2 \oplus B_3$

B_1B_0 \ B_3B_2	00	01	11	10
00	m0 0	m4 0	m12 1	m8 1
01	m1 0	m5 0	m13 1	m9 1
11	m3 0	m7 0	m15 1	m11 1
10	m2 0	m6 0	m14 1	m10 1

$G_3 = B_3$



logic circuit using XOR circuits

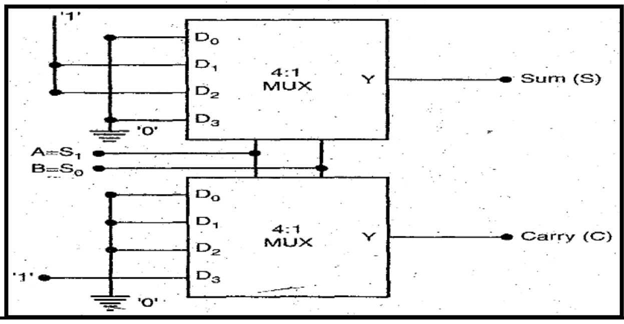
Question 4 This question is attributed with ***7 marks*** if answered properly; the answers are the following:

a) *(2.5 marks)*

Solution

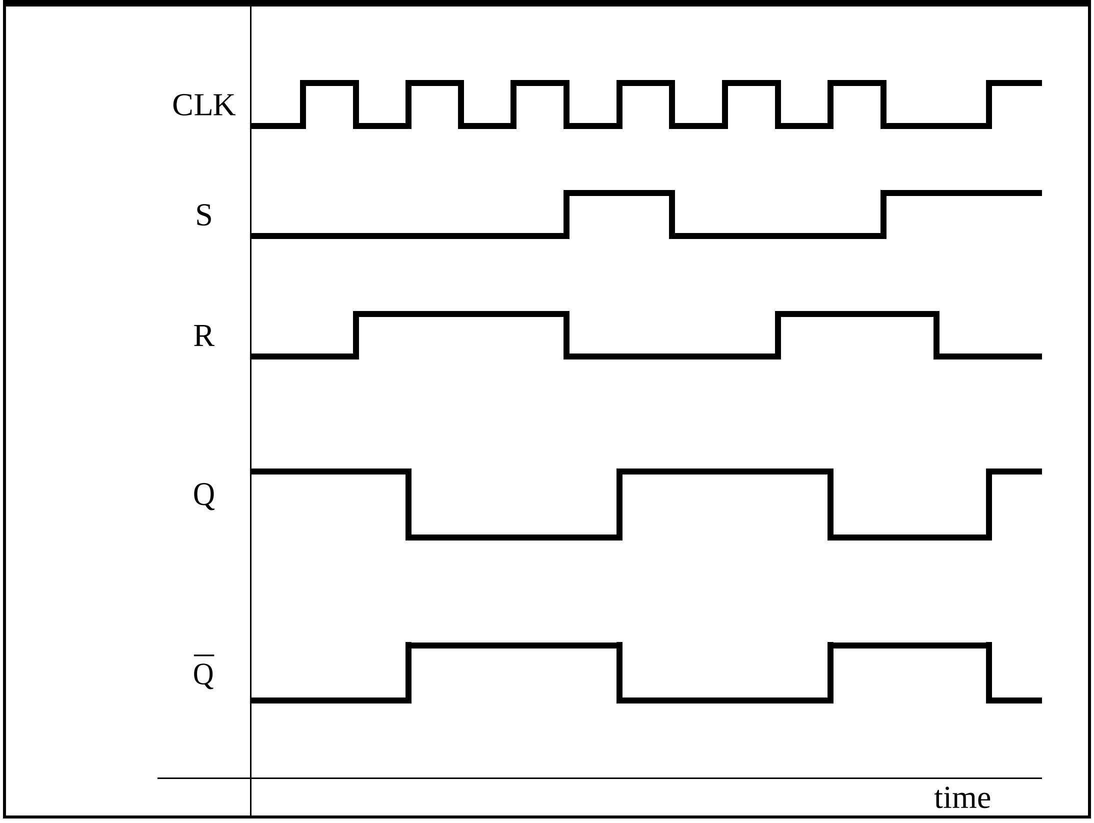
Truth table of half adder is as shown:

Inputs		Outputs	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



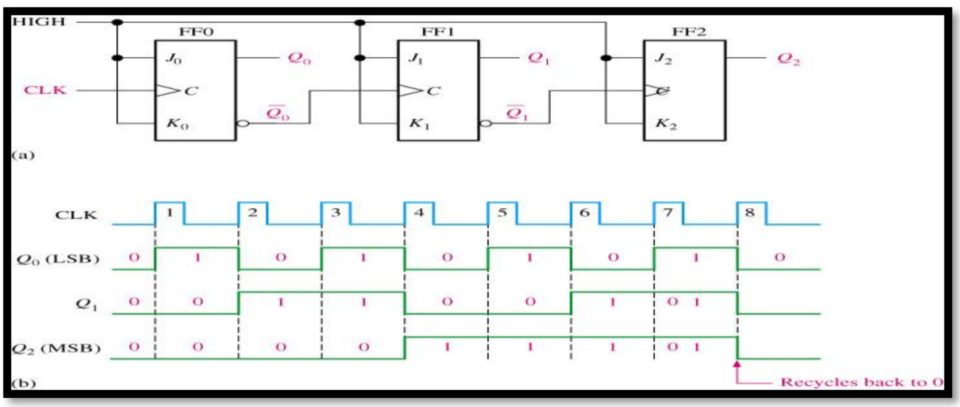
b) *(2 marks)*

Solution



c) *(2.5 marks)*

Solution



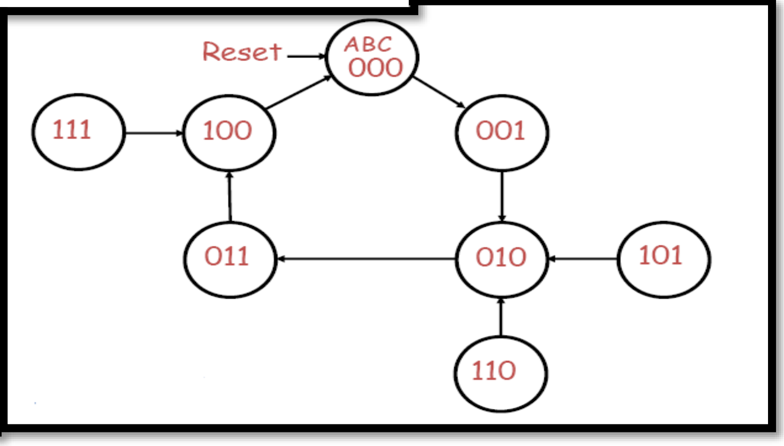
Question 5 This question is attributed with ***5 marks*** if answered properly; the answers are the following:

Solution

✓ Equations

- $A(t+1) = BC$ $\quad Z = A$
- $B(t+1) = B'C + BC'$
- $C(t+1) = A'C'$

A B C	A'B'C'	Z
0 0 0	0 0 1	0
0 0 1	0 1 0	0
0 1 0	0 1 1	0
0 1 1	1 0 0	0
1 0 0	0 0 0	1
1 0 1	0 1 0	1
1 1 0	0 1 0	1
1 1 1	1 0 0	1



Question 6 This question is attributed with ***6 marks*** if answered properly; the answers are the following:

Solution

Quick table:

Present-state			Next-state		
Q_2	Q_1	Q_0	Q_{2+}	Q_{1+}	Q_{0+}
0	0	1	0	1	1
0	1	1	0	1	0
0	1	0	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1
1	0	1	0	0	1

Full table:

Present-state			Next-state		
Q_2	Q_1	Q_0	Q_{2+}	Q_{1+}	Q_{0+}
0	0	0	x	x	x
0	0	1	0	1	1
0	1	0	1	1	0
0	1	1	0	1	0
1	0	0	x	x	x
1	0	1	0	0	1
1	1	0	1	1	1
1	1	1	1	0	1

Present-state			Next-state			Flip-flop input		
Q_2	Q_1	Q_0	Q_{2+}	Q_{1+}	Q_{0+}	T_2	T_1	T_0
0	0	1	0	1	1	0	1	0
0	1	1	0	1	0	0	0	1
0	1	0	1	1	0	1	0	0
1	1	0	1	1	1	0	0	1
1	1	1	1	0	1	0	1	0
1	0	1	0	0	1	1	0	0

Q_2 \ Q_1Q_0	T_2: 00	01	11	10	T_1: 00	01	11	10	T_0: 00	01	11	10
0	x	0	0	1	x	1	0	0	x	0	1	0
1	x	1	0	0	x	0	1	0	x	0	0	1

$T_2 = Q_2'Q_0' + Q_2Q_1'$ $\quad T_1 = Q_2'Q_1' + Q_2Q_1Q_0$ $\quad T_0 = Q_2Q_0' + Q_2'Q_1Q_0$