Philadelphia University
Faculty of Engineering

Marking Scheme

Exam Paper

BSc CE

Logic Circuits (630211)

Second Exam | First semester | Date 23/12/2018

Section 1

Weighting 20% of the module total

Lecturer:	Dr. Qadri Hamarsheh
Coordinator:	Dr. Qadri Hamarsheh
Internal Examiner:	Eng. Anis Nazer

Marking Scheme

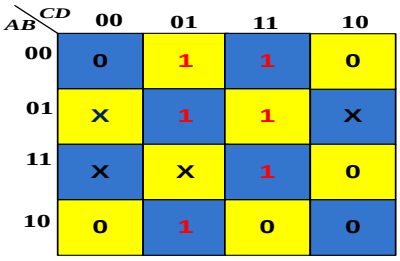
Logic Circuits (630211)

The presented exam questions are organized to overcome course material through 4 questions.
The *all questions* are compulsory requested to be answered.

Marking Assignments

Question 1 **Multiple Choice** ***(6 marks)***

1) The Boolean function **F** with don't-care conditions are represented in the **K-map** for four-variables as shown below, the simplification of the function F in **sum-of-products form** is:



a) $\bar{A}\,D + \bar{A}\,B + B\,D + \bar{C}\,D$
b) $\bar{A}\,D + \bar{A}\,B + \bar{C}\,D + A\,\bar{B}\,\bar{C}\,D$
c) $\bar{A}\,D + B\,D + \bar{C}\,D$
d) $\bar{A}\,\bar{B}\,D + \bar{A}\,B + B\,D + A\,\bar{B}\,\bar{C}\,D$

2) The simplified expression of half adder **carry** is

a) $c = xy + x$ **b)** $c = xy$
c) $c = xy + y$ **d)** $c = y + x$

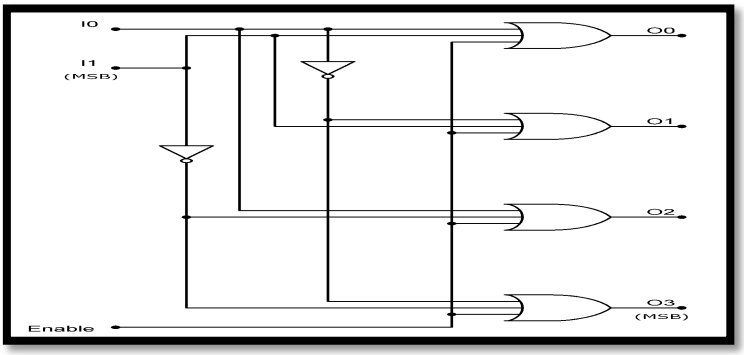
3) How many select lines will a **16 to 1 multiplexer** will have:

a) **4** **b)** **3**
c) **5** **d)** **6**

4) Decoder with enable input can be used as:

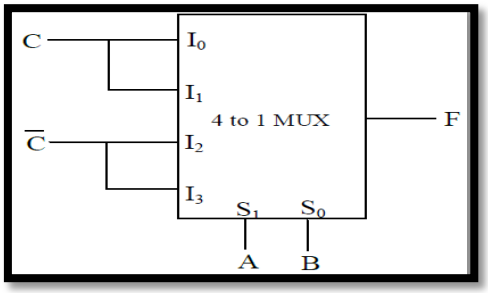
a) **Encoder** **b)** **Multiplexer**
c) **XOR** **d)** **Demultiplexer**

5) The following circuit is a _____.



a) **2-4 decoder with active low enable and active low outputs**
b) **2-4 decoder with active low enable and active high outputs**
c) **2-4 decoder with active high enable and active low outputs**
d) **2-4 decoder with active high enable and active high outputs**

6) The logic realized by the circuit shown in figure is

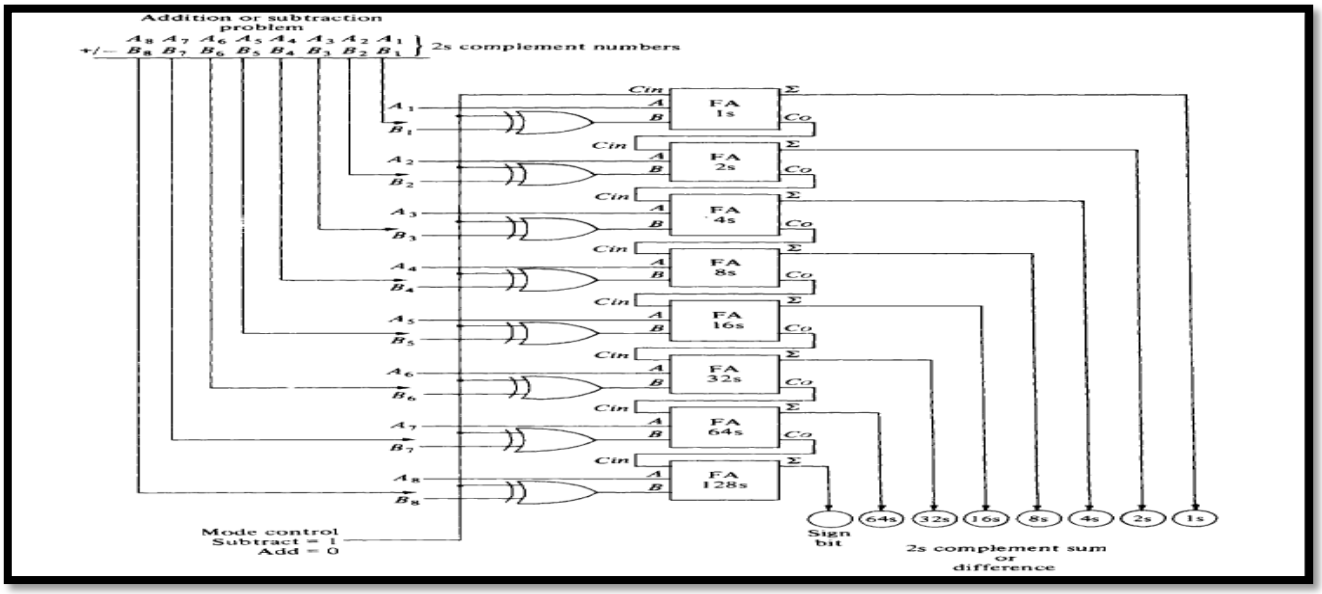


a) $F = B \oplus C$ **b)** $F = \overline{B \oplus C}$
c) $F = A \oplus C$ **d)** $F = \overline{A \oplus C}$

Question 2: *(5 marks)*

a) *(2.5 marks)*

Solution



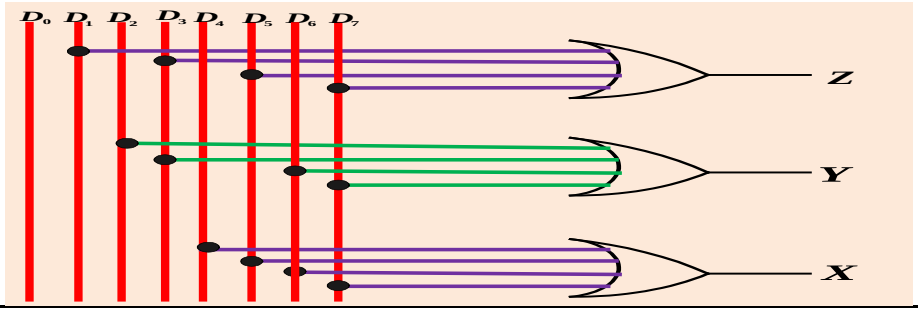
b) *(2.5 marks)*

Solution

An encoder is a digital circuit that performs the inverse operation of a decoder. An encoder has 2^n (or fewer) input lines and n output lines.

Inputs								*Outputs*		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	X	Y	Z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

$$X = D_4 + D_5 + D_6 + D_7$$
$$Y = D_2 + D_3 + D_6 + D_7$$
$$Z = D_1 + D_3 + D_5 + D_7$$

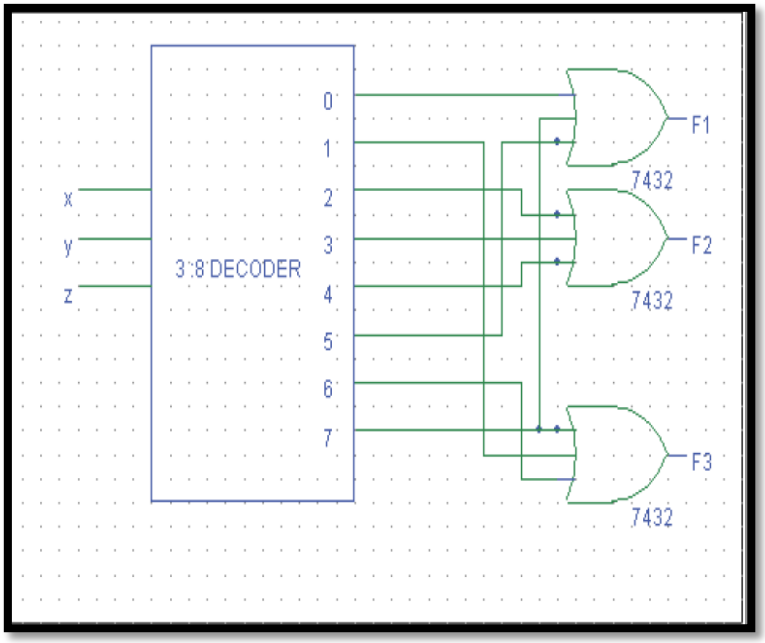


Question 3: ***(6 marks)***

a) ***(3 marks)***

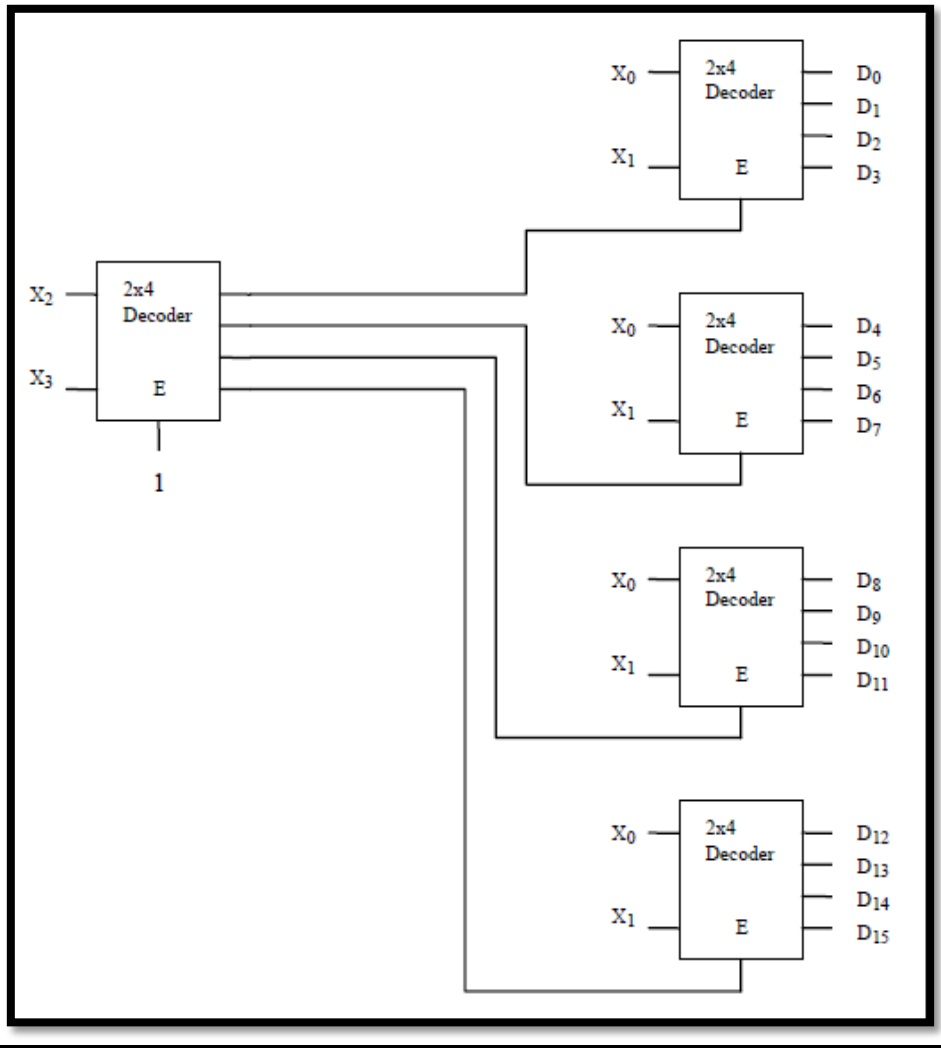
Solution

$$F1 = x'y'z' + xz(y + y') = x'y'z' + xyz + xy'z = \Sigma m(0,5,7)$$
$$F2 = \Sigma m(2,3,4)$$
$$F3 = \Sigma m(1,6,7)$$



b) ***(3 marks)***

Solution



Question 4: ***(3 marks)***

Solution