



Philadelphia University
Faculty of Engineering

Marking Scheme

Exam Paper

BSc CE

Logic Circuits (630211)

Second Exam

Second semester

Date 01/05/2019

Section 1

Weighting 20% of the module total

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Marking Scheme Logic Circuits (630211)

The presented exam questions are organized to overcome course material through 4 questions. The *all questions* are compulsory requested to be answered.

Marking Assignments

Question 1 Multiple Choice

(6 marks)

- 1) **BCD to 7 segments** is

a) encoder	b) mux
c) decoder	d) demux
- 2) To implement **binary full adder** using **decoders** we need:

a) 3-to-8 active high decoder with one AND logic gate	b) 3-to-8 active high decoder with two AND logic gates
c) 3-to-8 active high decoder with one OR logic gate	d) 3-to-8 active high decoder with two OR logic gates
- 3) The **carry propagation** in binary full adder can be expressed as _____.

a) $C_p = AB$	b) $C_p = A + B$
c) $C_p = A \oplus B$	d) $C_p = A \oplus \bar{B}$
- 4) **Encoders 3x8** are made by three

a) AND gate	b) OR gate
c) XOR gate	d) NAND gate
- 5) If the input combination **S=1, R=1** is applied to **NOR Based SR Latch** circuit, the (steady state) output will be:

a) Q=0, Q'=0	b) Q=0, Q'=1
c) Q=1, Q'=0	d) Q=1, Q'=1
- 6) Flip flop is:

a) level sensitive	b) Edge sensitive
c) Both of a and b	d) None of the above

Question 2:

(3 marks)

Solution

The demultiplexer is a combinational logic circuit that performs the **reverse operation** of multiplexer (Several output lines, one input line).

Internal logic circuit for 1-4 DEMUX

Solution

Truth table

Decimal digit	Input BCD code				Output Excess-3			
	A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0
10	1	0	1	0	X	X	X	X
11	1	0	1	1	X	X	X	X
12	1	1	0	0	X	X	X	X
13	1	1	0	1	X	X	X	X
14	1	1	1	0	X	X	X	X
15	1	1	1	1	X	X	X	X

The logic diagram illustrates the implementation of the Excess-3 code using a 4x16 decoder. The decoder has four inputs (A, B, C, D) and 16 outputs (0-15). The outputs are connected to four OR gates to produce the Excess-3 outputs W, X, Y, and Z. The connections are as follows:

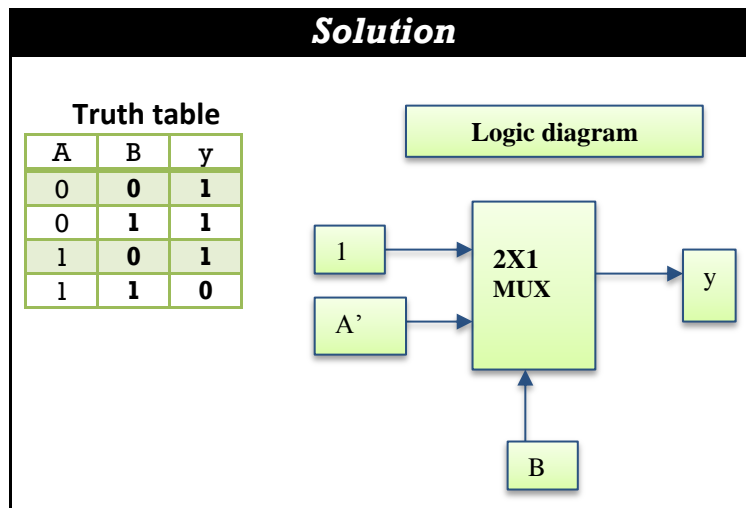
- W:** OR of decoder outputs 0, 1, 2, 3, 4, 5, 6, 7.
- X:** OR of decoder outputs 1, 2, 3, 4, 5, 6, 7, 8.
- Y:** OR of decoder outputs 2, 3, 4, 5, 6, 7, 8, 9.
- Z:** OR of decoder outputs 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15.

Question 4:

(5 marks)

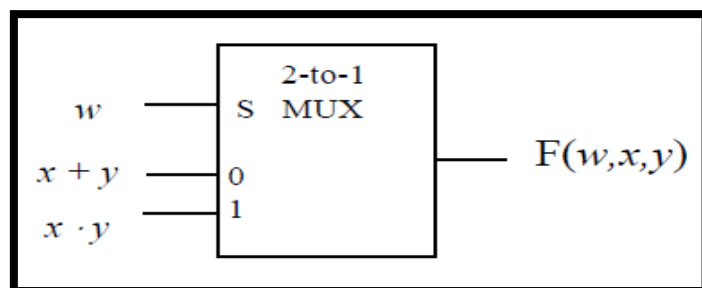
a)

(3 marks)



b)

(2 marks)



Solution

$$F(w, x, y) = \bar{w}x + \bar{w}y + xy$$