Philadelphia University
Faculty of Engineering

Marking Scheme

Quiz Paper

BSc CE

Microprocessors (0630313)

First Quiz Second semester Date: 12/03/2019

Section 1

Weighting 5% of the module total

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Marking Assignments

Question 1 This question is attributed with 5 marks if answered properly; the answers are as following:

1) A **20-bit address bus** allows access to a memory of capacity
   a) 1 MB
   b) 32MB
   c) 2 MB
   d) 64 MB

2) **Pipelining** improves CPU performance due to
   a) reduced memory access time
   b) the introduction of parallellism
   c) increased clock speed
   d) additional functional units

3) In the Intel architecture, there are actually several buses connecting the CPU to the rest of the computer. Which of the following is **not such a bus?**
   a) The control bus
   b) The logic bus
   c) The data bus
   d) The address bus

4) Which flags are NOT used for mathematical operations?
   a) Carry, Interrupt and Trap flag
   b) Direction, Interrupt and Sign flag
   c) Direction, Overflow and Trap flag
   d) Direction, Interrupt and Trap flag

5) If CS = 020AH, SS = 0801H, SI = 0100H and IP = 1BCDH the address of the next instruction is:
   a) 03C6D
   b) 03C70
   c) 03D5D
   d) None of the above