Philadelphia University





Student Name: Student Number: Serial Number:

Second Exam, First Semester: 2018/2019 Dept. of Computer Engineering

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Course Title:	Logic Circuits	Date:	23/12/2017
Course No:	630211	Time Allowed:	50 minutes
Lecturer:	Dr. Qadri Hamarsheh	No. Of Pages:	5

Instructions:

- **ALLOWED**: pens and drawing tools (**no red color**).
- NOT ALLOWED: Papers, literatures and any handouts. Otherwise, it will lead to the non-approval of your examination.
- Shut down Telephones, and other communication devices.

Please note:

- This exam paper contains 4 questions totaling 20 marks
- Write your name and your matriculation number on every page of the solution sheets.
- All solutions together with solution methods (explanatory statement) must be inserted in the labelled position on the solution sheets.
- You can submit your exam after the first hour.

<u>Question 1</u> Multiple Choice

Identify the choice that best completes the statement or answers the question.

1) The Boolean function **F** with don't-care conditions are represented in the **K-map** for four-variables as shown below, the simplification of the function F in **sum-of-products form** is:

	00 ^d	01	11	10
00	0	1	1	ο
01	×	1	1	×
11	x	×	1	о
10	ο	1	ο	0

a)	$\overline{A} D + \overline{A} B + B D + \overline{C} D$
b)	$\overline{A} D + \overline{A} B + \overline{C} D + A \overline{B} \overline{C} D$
c)	$\overline{A} D + B D + \overline{C} D$
d)	$\overline{A}\overline{B}D + \overline{A}B + BD + A\overline{B}\overline{C}D$

2) The simplified expression of half adder **carry** is

	$a) \qquad c = xy + x$	b) $\mathbf{c} = \mathbf{x}\mathbf{y}$	
	$c) \qquad c = xy + y$	$\mathbf{d}) \qquad \mathbf{c} = \mathbf{y} + \mathbf{x}$	
3)	How many select lines will a 16 to 1 mm	ultiplexer will have:	
	a) 4	b) 3	
	c) 5	d) 6	
4)	Decoder with enable input can be used as	s:	
	a) Encoder	b) Multiplexer	
	c) XOR	d) Demultiplexe	er

(6 marks)

5) The following circuit is a



- a) 2-4 decoder with active low enable and active low outputs
- b) 2-4 decoder with active low enable and active high outputs
- c) 2-4 decoder with active high enable and active low outputs
- d) 2-4 decoder with active high enable and active high outputs
- 6) The logic realized by the circuit shown in figure is



Question 2	(5 marks)
a) Draw a diagram of an 8-bit adder/subtractor.	(2.5 marks)
Solution	
b) Explain the function of an encoder . Implement an encoder using cate	as (25 marks)
b) Explain the function of an encoder: implement an encoder using gate	2.3 <i>marks</i>
Solution	

Question 3

a) A combinational circuit has 3 outputs F1, F2 and F3

$\mathbf{F1} = \bar{\mathbf{x}} \bar{\mathbf{y}} \bar{\mathbf{z}} + \mathbf{xz}$	
$\mathbf{F2} = \mathbf{x}\overline{\mathbf{y}}\overline{\mathbf{z}} + \overline{\mathbf{x}}\mathbf{y}$	
$F3 = \bar{x} \bar{v} z + xv$	

F3 = x y z + xyDesign the circuit with a **decoder** and **external gates**.

Solution

b) Design a 4-to-16 line decoder with Enable input using five 2-to-4 line decoders with Enable inputs. (3 marks)

Solution

<u>Question 4</u> (3 marks) Implement the following Boolean function with an **8-to-1 multiplexer** and a **single inverter** with **variable B** as an input.

$$f(A, B, C, D) = \Sigma m(2, 4, 6, 9, 10, 11, 15)$$

Solution

GOOD LUCK