Philadelphia University

Faculty of Engineering

Student Name:	
Student Number:	
Serial Number:	

Second Exam, Second Semester: 2018/2019
Dept. of Computer Engineering

Course Title:	**Logic Circuits**	**Date:**	01/05/2019
Course No:	**630211**	**Time Allowed:**	50 minutes
Lecturer:	Dr. Qadri Hamarsheh	**No. Of Pages:**	4

Instructions:

- **ALLOWED**: pens and drawing tools (**no red color**).
- **NOT ALLOWED**: Papers, calculators, literatures and any handouts. Otherwise, it will lead to the non-approval of your examination.
- **Shut down** Telephones, and other communication devices**.**

Please note:

- *This exam paper contains 4 questions totaling 20 marks*
- *Write your name and your matriculation number on every page of the solution sheets.*
- *All solutions together with solution methods (explanatory statement) must be inserted in the labelled position on the solution sheets.*
- *You can submit your exam after the first hour.*

Question 1 ***Multiple Choice*** ***(6 marks)***

Identify the choice that best completes the statement or answers the question.

1) **BCD** to **7 segments** is

a) **encoder** **b)** **mux**
c) **decoder** **d)** **demux**

2) To implement **binary full adder** using **decoders** we need:

a) **3-to-8 active high decoder with one AND logic gate**
b) **3-to-8 active high decoder with two AND logic gates**
c) **3-to-8 active high decoder with one OR logic gate**
d) **3-to-8 active high decoder with two OR logic gates**

3) The **carry propagation** in binary full adder can be expressed as _____.

a) $\mathbf{C_p = AB}$ **b)** $\mathbf{C_p = A + B}$
c) $C_p = A \oplus B$ **d)** $C_p = A \oplus \overline{B}$

4) **Encoders 3x8** are made by three

a) **AND gate** **b)** **OR gate**
c) **XOR gate** **d)** **NAND gate**

5) If the input combination **S=1, R=1** is applied to **NOR** Based **SR** Latch circuit, the (steady state) output will be:

a) **Q=0, Q'=0** **b)** **Q=0, Q'=1**
c) **Q=1, Q'=0** **d)** **Q=1, Q'=1**

6) Flip flop is:

a) **level sensitive** **b)** **Edge sensitive**
c) **Both of a and b** **d)** **None of the above**

Question 2 ***(3 marks)***

Explain the working of a **demultiplexer** with the help of the logic circuit

Solution

Question 3: ***(6 marks)***

Design **BCD to Excess-3** code converter using **decoder 4x16**.

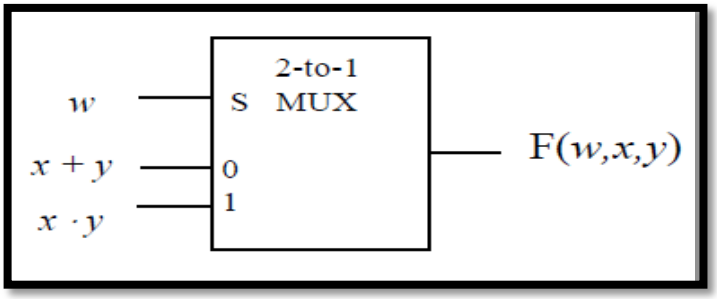
Solution

Question 4: *(5 marks)*

a) Implement **2 input NAND** gate function using a **2:1 multiplexer.** *(3 marks)*

Solution

b) Find the Boolean function **F(w, x, y)** and express it in the simplified **SOP** format. *(2 marks)*



Solution

GOOD LUCK