Philadelphia University

Faculty of Engineering

Student Name:	
Student Number:	
Serial Number:	

Second Exam, First Semester: 2019/2020
Dept. of Computer Engineering

Course Title:	**Logic Circuits**	**Date:**	02/01/2020
Course No:	**630211**	**Time Allowed:**	50 minutes
Lecturer:	Dr. Qadri Hamarsheh	**No. Of Pages:**	4

Instructions:

- **ALLOWED**: pens and drawing tools (**no red color**).
- **NOT ALLOWED**: Papers, calculators, literatures and any handouts. Otherwise, it will lead to the non-approval of your examination.
- **Shut down** Telephones, and other communication devices**.**

Please note:

- *This exam paper contains 4 questions totaling 20 marks*
- *Write your name and your matriculation number on every page of the solution sheets.*
- *All solutions together with solution methods (explanatory statement) must be inserted in the labelled position on the solution sheets.*

Question 1 ***Multiple Choice*** ***(5 marks)***

Identify the choice that best completes the statement or answers the question.

1) The **sum** of ripple carry adder is

a) $S_i = A_i \oplus B_i \oplus C_i$
b) $S_i = A_i B_i + A_i C_i + B_i C_i$
c) $S_i = A_i + B_i + C_i$
d) $S_i = A_i B_i C_i$

2) A **BCD-to-7 segment decoder** has **0100** on its inputs. The active outputs are

a) **a, c, f; g** **b)** **b, c, f; g**
c) **b, c, e, f** **d)** **b, d, e, g**

3) A **6x64** line decoder can be built using:

a) **six 2x4 line decoders only** **b)** **nine 2x4 line decoders only**
c) **seven 3x8 line decoders only** **d)** **nine 3x8 line decoders only**

4) A **demultiplexer** can be used as

a) **Encoder** **b)** **Multiplexer**
c) **Decoder** **d)** **None of the above**

5) An **8-to-1** multiplexer has inputs **A, B** and **C** connected to the selection inputs **S2, S1** and **S0**, respectively. The data inputs I_0 through I_7 are as follows:

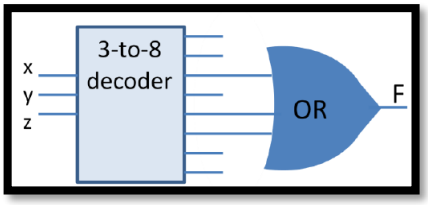
$I_1 = I_2 = 0$; $I_3 = I_5 = I_7 = 1$; $I_0 = I_4 = \bar{D}$ **and** $I_6 = D$

The **Boolean function** that the multiplexer implements is:

a) $F = \Sigma m\,(0, 6, 7, 8, 10, 11, 13, 14, 15)$
b) $F = \Sigma m\,(1, 2, 3, 4, 5, 9, 12)$
c) $F = \Sigma m\,(0, 6, 7, 8, 9, 11, 13, 14, 15)$
d) $F = \Sigma m\,(0, 6, 7, 9, 11, 14, 15)$

Question 2 ***(7 marks)***

a) What function $F(x, y, z)$ is implemented in the figure shown below? You may answer using the minterm notion. ***(2 marks)***



Solution

b) A combinational circuit is defined by the following three Boolean functions: ***(5 marks)***

$$\mathbf{F1} = \overline{\mathbf{X} + \mathbf{Y}} + \mathbf{XYZ}$$

$$F2 = \overline{XZ}\,Y$$

$$F3 = \overline{\overline{X} + Y} + \overline{X}\overline{Y}\overline{Z}$$

Design the circuit with a **3-to-8 decoder** and **external** gates.

Solution

Question 3: ***(5 marks)***

Design the function $\mathbf{F(A, B, C, D)} = \sum \mathbf{m}\ (\mathbf{1, 4, 5, 8, 10, 12, 13})$ using **8x1multiplexer**.

Solution

Question 4 ***(3 marks)***

Construct a **1-to-32 demultiplexer** using only two types of **demultiplexers**: **1-to-4 and 1-to-8**.

Solution

GOOD LUCK