Philadelphia University

Faculty of Engineering



Student Name:

Student Number:

Dept. of Computer Engineering

First Quiz, Second Semester: 2018/2019

Course Title:	Microprocessors	Date:	12/03/2019
Course No:	0630313	Time Allowed:	10 minutes
Lecturer:	Dr. Qadri Hamarsheh	No. Of Pages:	1

Information for candidates

- 1. This Quiz paper contains 1 question totaling 5 marks
- 2. The marks for parts of question are shown in round brackets.

Advices to candidates

- 1. You should attempt all sub questions.
- 2. You should write your answers clearly.

<u>Question 1</u> Multiple Choice

Identify the choice that best completes the statement or answers the question

- 1) A **20-bit address bus** allows access to a memory of capacity
 - a) 1 MB b) 32MB
 - c) 2 MB d) 64 MB
- 2) **Pipelining** improves CPU performance due to
 - a) reduced memory access time
 - c) increased clock speed
- 3) In the Intel architecture, there are actually several buses connecting the CPU to the rest of the computer.

d)

Which of the following is **not such a bus?**

- a) The control bus
- c) The data bus

- b) The logic bus
- d) The address bus

b) the introduction of parallelism

additional functional units

- 4) Which flags are NOT used for mathematical operations?
 - a) Carry, Interrupt and Trap flag
 - b) Direction, Interrupt and Sign flag
 - c) Direction, Overflow and Trap flag
 - d) Direction, Interrupt and Trap flag
- 5) If CS = 020AH, SS = 0801H, SI = 0100H and IP = 1BCDH the address of the next instruction is:
 - a) 03C6D
 - b) 03C70
 - c) 03D5D
 - d) None of the above

GOOD LUCK

(5 marks)