Philadelphia University
Faculty of Engineering
Department of Computer
First semester, 2009/2010

Course Syllabus

Course Title: Logic Circuits	**Course code: 630261**
Course Level: 2nd year	**Course prerequisite (s) and/or corequisite (s): 710101**
Lecture Time: 12:10 – 13:00	**Credit hours: 3**

Academic Staff Specifics

Name	Rank	Office Number and Location	Office Hours	E-mail Address
Dr. Ali Khwaldeh	Assistanc Professor	E710	9-10 Mon. 10-11 Wed	akhwaldeh@philadelphia.edu.j

Course module description:
This class is an introduction to the basic concepts, analysis, and design of digital systems. This consists of both combinational and sequential logic. Lectures will enable students to experience with several levels of digital systems.

Course module objectives:
At Completing of this module the student should be able to:

- Design methodologies for electronic circuits, to use mathematical expressions to describe the functions of simple combinational and sequential circuits.
- Convert numerical data from one format to another and to use different formats to represent numerical data.
- Understand Boolean algebra, basic laws and rules in logic design, DeMorgan's theorem, Karnaugh map, and approaches to simplifying logic circuits.
- Understand systematical design methodology for combinational logic circuits and build this kind of digital systems by using some IC devices.
- Understand systematical design methodology for sequential logic circuits.

Course/ module components

- **Books (title , author (s), publisher, year of publication)**

  (Text Book) Digital Design, 4th Edition, M. Morris Mano and Michael D. Ciletti, Prentice Hall, 2007.

- **Support material (s) (Course website: Includes reference books and Course Notes_ Power Point Slides). http://lbadri.com/index.php?option=com_content&task=view&id=29&Itemid=33**
- **Study guide (s)**
- **Homework and laboratory guide (s): Listed in the Course website.**

Teaching methods:

Lectures, tutorials, and problem solving.

Learning outcomes:

- Knowledge and understanding

  - Ability to analyze and understand the behavior of combinational and sequential digital circuits.
  - Ability to map and minimize Boolean functions as well as represent them in various standard forms.
  - Ability to design and implement combinational and sequential logic circuits.
  - Understanding of various combinational "building blocks" such as decoders, multiplexers, and encoders.
  - Ability to design and implement arithmetic logic circuits.
  - Understanding of the behavior exhibited by latches and flip-flops.
  - Ability to design and implement sequential circuits.
  - Understanding of various sequential "building blocks" such as counters and shift registers

- Cognitive skills (thinking and analysis)

  - Ability to analyze the behavior of digital circuits.
  - Ability to design and implement combinational logic circuits.
  - Understanding of various combinational "building blocks" such as decoders, multiplexers, and encoders.
  - Ability to design and implement arithmetic logic circuits.
  - Ability to design and implement sequential circuits.
  - Understanding of various sequential "building blocks" such as counters and shift registers.

- Communication skills (personal and academic).

  - Ability to search appropriate literature and other scientific resources for problem formulation, analysis and design.
  - Ability for using appropriate mathematical tools (software, hardware and mathematical algorithms) for the solution of related problems in computer systems engineering.
  - Ability for engineering thinking in analyzing the behavior of digital circuits and its design.

- Practical and subject specific skills (Transferable Skills).

  - Ability to map and minimize Boolean functions as well as represent them in various standard forms.
  - Ability to design and implement combinational logic circuits.
  - Understanding of various combinational "building blocks" such as decoders, multiplexers, and encoders.
  - Ability to design and implement arithmetic logic circuits.

- Ability to design and implement sequential circuits.
- Understanding of various sequential "building blocks" such as counters and shift registers.

Course Intended Learning Outcomes							
A - Knowledge and Understanding							
A1.	A2.	A3.	A4.	A5.	A6.	A7.	A8.
■	■				■		
B - Intellectual Skills							
B1.	B2.	B3.	B4.	B5.	B6.	B7.	B8.	B9.
■	■	■		■		■	
C - Practical Skills							
C1.	C2.	C3.	C4.	C5.	C6.	C7.	C8.	C9.	C10.
			■	■					■
D - Transferable Skills						
D1.	D2.	D3.	D4.	D5.	D6.	D7.
	■	■		■	■	

Assessment instruments

- Short reports and/ or presentations, and/ or Short research projects
- Quizzes.
- Home works
- Final examination: 50 marks

Allocation of Marks	
Assessment Instruments	**Mark**
First exam	**20%**
Second exam	**20%**
Final examination: 50 marks	**50%**
Reports, research projects, Quizzes, Home works, Projects	**10%**

Documentation and academic honesty

- Documentation style (with illustrative examples)

- Protection by copyright
- Avoiding plagiarism.

Course/module academic calendar

week	Basic and support material to be covered	Homework/reports and their due dates
(1)	Course Overview	
(2)	Introduction to Digital Systems. Number Systems and Conversions	
(3)	Boolean Algebra and Logic Gates	Assingment1 Week 4
(4)	Minimization Methods and Don't care conditions	Assingment2 Week 5
(5)	Representation and implementation of Boolean circuits using other logic gates.	Assingment3 Week 6
(6)	Tutorials, review and study guide of first exam material	
(7) **First examination**	Analysis Procedure of combinational circuits	
(8)	Combinational Circuits design, BCD Display	Assingment4 Week 9
(9)	Adder and Subtractor, Magnitude comparators,	Assingment5 Week 10
(10)	Multiplexers, Encoders, and Decoders.	
(11)	Tutorials, review and study guide of second exam material	Assingment6 Week 12
(12) **Second examination**	Sequential Circuits: Latches and Flip flops	Assingment7 Week 13
(13)	Analyzing Sequential Circuits, Finite State Machine Design Procedure. State Reduction and Assignment	Assingment8 Week 14
(14)	Shift Registers, Counters, And Timing Analysis.	Assingment9 Week 15
(15) **Specimen examination (Optional)**	Tutorials, review and study guide of final exam material	
(16) **Final Examination**		

Expected workload:

On average students need to spend 2 hours of study and preparation for each 50-minute lecture/tutorial.

Attendance policy:

Absence from lectures and/or tutorials shall not exceed 15%. Students who exceed the 15% limit without a medical or emergency excuse acceptable to and approved by the Dean of the relevant college/faculty shall not be allowed to take the final examination and shall receive a mark of zero for the course. If the excuse is approved by the Dean, the student shall be considered to have withdrawn from the course.

Module references

Books

1. Practical Digital Logic Design and Testing, P. K. Lala, Prentice Hall, 1996.
2. Introduction to Digital Logic Design, J. P. Hayes, Addison-Wesley, 1996.
3. Digital Electronics: Principles and Applications, R. L. Tokheim, 5th Edition, McGraw-Hill, 2000.

Web sites

http://lbadri.com
http://www.digikey.com
http://www.edaboard.com/forums.html