

## Philadelphia University Faculty of Information Technology Department of Computer Science ----- Semester, 2007/2008

# Course Syllabus

Course Title: Computer Logic Design	Course code: 750131
Course Level: 1	Course prerequisite(s) and/or corequisite(s): 710101
Lecture Time:	Credit hours: 3

## Academic Staff Specifics

Name	Rank	Office Number and Location	Office Hours	E-mail Address

## **Course Description:**

This module introduces the concepts of the design and implementation of digital circuits. Laboratory experiments will be used to reinforce the theoretical concepts discussed in lectures. The lab experiments will involve the design and implementation of digital circuits. Emphasis is on the use computer aided tools in the design, simulation, and testing of digital circuits.

## **Course Objectives:**

The aim of the module is to introduce to the students the topics that include combinational and sequential circuit analysis and design, digital circuit design optimization methods using random logic gates, multiplexers, decoders, registers, counters and programmable logic arrays.

## **Course Components**

- Introduction to Digital logic Design
- Binary Systems and Codes
- Binary Codes: BCD, Gray, ASCII and EBCDIC
- Binary Logic and Logic Gates: AND, OR and NOT
- Boolean Algebra and Logic Gates
- Integrated Circuits
- Gate-Level Minimization
- Analysis and Synthesis of Combinational Circuits
- Analysis and Synthesis of Sequential Circuits
- Registers and Counters
- Sequential Circuits with Programmable Logic Devices

## <u>Textbook:</u> Title: Digital Logic Author: Morris Mano Publisher: Prentice Hall, 1991 or 2002

In addition to the above, the students will be provided with handouts by the lecturer.

## **Teaching Methods:**

Duration: 16 weeks, 48 hours in total Lectures: 41 hours (2-3 per week) Tutorial: 4 hours (1 every 3 weeks) Laboratory: 3 hours.

#### **Learning Outcomes:**

## • Knowledge and understanding

- Minimize functions using any type of minimizing algorithms (Boolean algebra, Karnaugh map or Tabulation Method).
- Cognitive skills (thinking and analysis).
  - Define the problem (Inputs and Outputs), write its functions.
  - Implement functions using digital circuit (Combinational or Sequential).

#### • Communication skills (personal and academic).

- Have knowledge in analyzing and designing procedures of Combinational and Sequential circuits.

#### • Practical and subject specific skills (Transferable Skills).

- Work effectively with others.
- Use simulation software, for testing the designed circuit.

#### Assessment Instruments

Allocation of Marks		
Assessment Instruments	Mark	
First examination	15%	
Second examination	15%	
Final Exam (written unseen exam)	50%	
Reports, assignments, Quizzes, Home works, Tutorials	20%	
Total	100%	

\* Make-up exams will be offered for valid reasons only with consent of the Dean. Make-up exams may be different from regular exams in content and format.

#### **Practical Submissions**

The assignments that have work to be assessed will be given to the students in separate documents including the due date and appropriate reading material.

## **Documentation and Academic Honesty**

Submit your home work covered with a sheet containing your name, number, course title and number, and type and number of the home work (e.g. tutorial, assignment, and project).

Any completed homework must be handed in to my office (room IT...) by 15:00 on the due date. After the deadline "zero" will be awarded. You must keep a duplicate copy of your work because it may be needed while the original is being marked.

You should hand in with your assignments:

- 1- A printed listing of your test programs (if any).
- 2- A brief report to explain your findings.
- 3- Your solution of questions.

#### • Protection by Copyright

- 1. Coursework, laboratory exercises, reports, and essays submitted for assessment must be your own work, unless in the case of group projects a joint effort is expected and is indicated as such.
- 2. Use of quotations or data from the work of others is entirely acceptable, and is often very valuable provided that the source of the quotation or data is given. Failure to provide a source or put quotation marks around material that is taken from elsewhere gives the appearance that the comments are ostensibly your own. When quoting word-for-word from the work of another person quotation marks or indenting (setting the quotation in from the margin) must be used and the source of the quoted material must be acknowledged.
- 3. Sources of quotations used should be listed in full in a bibliography at the end of your piece of work.

#### • Avoiding Plagiarism.

- 1. Unacknowledged direct copying from the work of another person, or the close paraphrasing of somebody else's work, is called plagiarism and is a serious offence, equated with cheating in examinations. This applies to copying both from other students' work and from published sources such as books, reports or journal articles.
- 2. Paraphrasing, when the original statement is still identifiable and has no acknowledgement, is plagiarism. A close paraphrase of another person's work must have an acknowledgement to the source. It is not acceptable for you to put together unacknowledged passages from the same or from different sources linking these together with a few words or sentences of your own and changing a few words from the original text: this is regarded as over-dependence on other sources, which is a form of plagiarism.
- 3. Direct quotations from an earlier piece of your own work, if not attributed, suggest that your work is original, when in fact it is not. The direct copying of one's own writings qualifies as plagiarism if the fact that the work has been or is to be presented elsewhere is not acknowledged.
- 4. Plagiarism is a serious offence and will always result in imposition of a penalty. In deciding upon the penalty the Department will take into account factors such as the year of study, the extent and proportion of the work that has been plagiarized, and the apparent intent of the student. The penalties that can be imposed range from a minimum of a zero mark for the work (without allowing resubmission) through caution to disciplinary measures (such as suspension or expulsion).

# Course Academic Calendar

Introduction to Digital logic Design.       Introduction to digital logic Design.         (2)       Binary Systems and Codes: Binary Numbers. Octal and Hexadecimal Numbers. Number Base Conversions. Arithmetic Operation with different Bases         (3)       Complements. Signed Binary Numbers. Binary Codes: BCD, Gray, ASCII and EBCDIC. Binary Logic and Logic Gates: AND, OR and NOT       Tutorial 1         (4)       Boolean Algebra and Logic Gates: Boolean Functions.       Lab 1         (5)       Standard Forms: Minterm and Maxterm. Simplification of Boolean Functions using SOP and POS.       Tutorial 2         (6)       Logic Operations: NAND, NOR, Exclusive-OR and Equivalence. Integrated Circuits       Tutorial 2         (7)       Gate-Level Minimization: The Map Method. Two- and Three-Variable Map. Four-Variable Map. Four-Variable Map. Product of Sums Simplification. Don't-Care Conditions.       Lab 2         (8)       NAND and NOR Implementation. The Tabulation Method. Simplification of Boolean Functions using Tabulation Method.       Lab 2	Week	Basic and support material to be	Homework/reports and their due dates
(1)       Binary Systems and Codes: Binary Numbers. Octal and Hexadecimal Numbers. Number Base Conversions. Arithmetic Operation with different Bases         (3)       Complements. Signed Binary Numbers. Binary Codes: BCD, Gray, ASCII and EBCDIC. Binary Logic and Logic Gates: AND, OR and NOT       Tutorial 1         (4)       Boolean Algebra and Logic Gates: Boolean Functions.       Lab 1         (5)       Standard Forms: Minterm and Maxterm. Simplification of Boolean Functions using SOP and POS.       Tutorial 2         (6)       Logic Operations: NAND, NOR, Exclusive-OR and Equivalence. Integrated Circuits       Tutorial 2         (7)       Gate-Level Minimization: First Exam       The Map Method. Two- and Three-Variable Map. Four-Variable Map. Product of Sums Simplification. Don't-Care Conditions.       Lab 2         (8)       NAND and NOR Implementation. Functions using Tabulation Method.       Lab 2         (9)       Analysis and Synthesis of Combinational Circuits: Or and Synthesis of Combinational Circuits:       Tutorial 3	(1)	Introduction to Digital logic Design	
<ul> <li>(2) Brinary Systems and Codes. Brinary Numbers. Octal and Hexadecimal Numbers. Number Base Conversions. Arithmetic Operation with different Bases</li> <li>(3) Complements. Binary Codes: BCD, Gray, ASCII and EBCDIC. Binary Logic and Logic Gates: AND, OR and NOT</li> <li>(4) Boolean Algebra and Logic Gates: Basic Definition. Basic Theorems. Boolean Functions.</li> <li>(5) Standard Forms: Minterm and Maxterm. Simplification of Boolean Functions using SOP and POS.</li> <li>(6) Logic Operations: NAND, NOR, Exclusive-OR and Equivalence. Integrated Circuits</li> <li>(7) Gate-Level Minimization: The Map Method. Two- and Three-Variable Map. Four-Variable Map. Product of Sums Simplification. Don't-Care Conditions.</li> <li>(8) NAND and NOR Implementation. The Tabulation Method. Simplification of Boolean Functions using Tabulation</li> <li>(9) Analysis and Synthesis of Combinational Circuits: On the function of Combinational Circuits:</li> </ul>	(1)	Binary Systems and Codes:	
Ortal and Hexadecimal Numbers.         Number Base Conversions.         Arithmetic Operation with different Bases         (3)       Complements.         Signed Binary Numbers.         Binary Codes: BCD, Gray, ASCII and         EBCDIC.         Binary Logic and Logic Gates: AND,         OR and NOT         (4)         Boolean Algebra and Logic Gates:         Lab 1         Basic Definition.         Basic Theorems.         Boolean Functions.         (5)       Standard Forms: Mintern and Maxterm.         Simplification of Boolean Functions using         SOP and POS.         (6)       Logic Operations: NAND, NOR,         Exclusive-OR and Equivalence.         Integrated Circuits         (7)       Gate-Level Minimization:         The Map Method.         Two- and Three-Variable Map.         Four-Variable Map.         Product of Sums Simplification.         Don't-Care Conditions.         (8)       NAND and NOR Implementation.         The Tabulation Method.         Simplification of Boolean         Functions using Tabulation         Method.         Simplification of Boolean         Functions using Tabulatio	(2)	Binary Numbers	
Number Base Conversions. Arithmetic Operation with different Bases         (3)       Complements. Signed Binary Numbers. Binary Codes: BCD, Gray, ASCII and EBCDIC. Binary Logic and Logic Gates: AND, OR and NOT       Tutorial 1         (4)       Boolean Algebra and Logic Gates: Basic Definition. Basic Theorems. Boolean Functions.       Lab 1         (5)       Standard Forms: Minterm and Maxterm. Simplification of Boolean Functions using SOP and POS.       Tutorial 2         (6)       Logic Operations: NAND, NOR, Exclusive-OR and Equivalence. Integrated Circuits       Tutorial 2         (7)       Gate-Level Minimization: The Map Method. Two- and Three-Variable Map. Four-Variable Map. Product of Sums Simplification. Don't-Care Conditions.       Lab 2         (8)       NAND and NOR Implementation. The Tabulation Method. Simplification of Boolean Functions using Tabulation Method.       Lab 2         (9)       Analysis and Synthesis of Combinational Circuits: Out of the function of Combinational Circuits:       Tutorial 3		Octal and Heyadecimal Numbers	
Arithmetic Operation with different Bases         (3)       Complements. Signed Binary Numbers. Binary Codes: BCD, Gray, ASCII and EBCDIC. Binary Logic and Logic Gates: AND, OR and NOT       Tutorial 1         (4)       Boolean Algebra and Logic Gates: Basic Definition. Basic Theorems. Boolean Functions.       Lab 1         (5)       Standard Forms: Minterm and Maxterm. Simplification of Boolean Functions using SOP and POS.       Tutorial 2         (6)       Logic Operations: NAND, NOR, Exclusive-OR and Equivalence. Integrated Circuits       Tutorial 2         (7)       Gate-Level Minimization: The Map Method. Two- and Three-Variable Map. Four-Variable Map. Product of Sums Simplification. Don't-Care Conditions.       Lab 2         (8)       NAND and NOR Implementation. The Tabulation of Boolean Functions using Tabulation Method.       Lab 2         (9)       Analysis and Synthesis of Combinational Circuits: On the function of Boolean Functions       Tutorial 3		Number Base Conversions	
(3)       Complements.       Tutorial 1         (3)       Complements.       Tutorial 1         Signed Binary Numbers.       Binary Codes: BCD, Gray, ASCII and EBCDIC.       Binary Logic and Logic Gates: AND, OR and NOT         (4)       Boolean Algebra and Logic Gates:       Lab 1         Basic Definition.       Basic Theorems.       Boolean Functions.         (5)       Standard Forms: Minterm and Maxterm.       Simplification of Boolean Functions using SOP and POS.         (6)       Logic Operations: NAND, NOR, Exclusive-OR and Equivalence. Integrated Circuits       Tutorial 2         (7)       Gate-Level Minimization:       The Map Method. Two- and Three-Variable Map. Four-Variable Map. Product of Sums Simplification. Don't-Care Conditions.         (8)       NAND and NOR Implementation. The Tabulation Method. Simplification of Boolean Functions using Tabulation Method.       Lab 2         (9)       Analysis and Synthesis of Combinational Circuits:       Tutorial 3		Arithmetic Operation with different Bases	
<ul> <li>(5) Competencies: Signed Binary Numbers. Binary Codes: BCD, Gray, ASCII and EBCDIC. Binary Logic and Logic Gates: AND, OR and NOT</li> <li>(4) Boolean Algebra and Logic Gates: Basic Definition. Basic Theorems. Boolean Functions.</li> <li>(5) Standard Forms: Minterm and Maxterm. Simplification of Boolean Functions using SOP and POS.</li> <li>(6) Logic Operations: NAND, NOR, Exclusive-OR and Equivalence. Integrated Circuits</li> <li>(7) Gate-Level Minimization: The Map Method. Two- and Three-Variable Map. Four-Variable Map. Product of Sums Simplification. Don't-Care Conditions.</li> <li>(8) NAND and NOR Implementation. The Tabulation Method. Simplification of Boolean Functions using Tabulation</li> <li>(9) Analysis and Synthesis of Combinational Circuits: On the integrate I of the time</li> </ul>	(3)	Complements	Tutorial 1
Binary Codes: BCD, Gray, ASCII and EBCDIC.         Binary Logic and Logic Gates: AND, OR and NOT         (4)       Boolean Algebra and Logic Gates: Basic Definition. Basic Theorems. Boolean Functions.         (5)       Standard Forms: Minterm and Maxterm. Simplification of Boolean Functions using SOP and POS.         (6)       Logic Operations: NAND, NOR, Exclusive-OR and Equivalence. Integrated Circuits         (7)       Gate-Level Minimization: The Map Method.         First Exam       The Map Method.         NAND and NOR Implementation. Don't-Care Conditions.       Lab 2         (8)       NAND and NOR Implementation. The Tabulation Method. Simplification of Boolean Functions using Tabulation Method.       Lab 2	(3)	Signed Binary Numbers	
Binary Logic and Logic Gates: AND, OR and NOT       Itab 1         (4)       Boolean Algebra and Logic Gates: Basic Definition. Basic Theorems. Boolean Functions.       Itab 1         (5)       Standard Forms: Minterm and Maxterm. Simplification of Boolean Functions using SOP and POS.       Tutorial 2         (6)       Logic Operations: NAND, NOR, Exclusive-OR and Equivalence. Integrated Circuits       Tutorial 2         (7)       Gate-Level Minimization: The Map Method. Two- and Three-Variable Map. Four-Variable Map. Product of Sums Simplification. Don't-Care Conditions.       Lab 2         (8)       NAND and NOR Implementation. The Tabulation Method.       Lab 2         (9)       Analysis and Synthesis of Combinational Circuits:       Tutorial 3		Binary Codes: BCD Gray ASCII and	
Binary Logic and Logic Gates: AND, OR and NOT       Image: Content of the system of the		FBCDIC	
OR and NOT         (4)       Boolean Algebra and Logic Gates: Basic Definition. Basic Theorems. Boolean Functions.       Lab 1         (5)       Standard Forms: Minterm and Maxterm. Simplification of Boolean Functions using SOP and POS.       Tutorial 2         (6)       Logic Operations: NAND, NOR, Exclusive-OR and Equivalence. Integrated Circuits       Tutorial 2         (7)       Gate-Level Minimization: The Map Method. Two- and Three-Variable Map. Four-Variable Map. Product of Sums Simplification. Don't-Care Conditions.       Lab 2         (8)       NAND and NOR Implementation. The Tabulation Method. Simplification of Boolean Functions using Tabulation Method.       Lab 2		Binary Logic and Logic Gates: AND	
(4)       Boolean Algebra and Logic Gates: Basic Definition. Basic Theorems. Boolean Functions.       Lab 1         (5)       Standard Forms: Minterm and Maxterm. Simplification of Boolean Functions using SOP and POS.       Tutorial 2         (6)       Logic Operations: NAND, NOR, Exclusive-OR and Equivalence. Integrated Circuits       Tutorial 2         (7)       Gate-Level Minimization: The Map Method. Two- and Three-Variable Map. Four-Variable Map. Product of Sums Simplification. Don't-Care Conditions.       Lab 2         (8)       NAND and NOR Implementation. The Tabulation Method. Simplification of Boolean Functions using Tabulation Method.       Lab 2         (9)       Analysis and Synthesis of Combinational Circuits:       Tutorial 3		OR and NOT	
(1)       Doritin Digital and Digital Gales.       Data 1         Basic Definition.       Basic Theorems.       Boolean Functions.         (5)       Standard Forms: Minterm and Maxterm.         Simplification of Boolean Functions using SOP and POS.       Tutorial 2         (6)       Logic Operations: NAND, NOR, Exclusive-OR and Equivalence.       Tutorial 2         (7)       Gate-Level Minimization:       Tutorial 2         First Exam       The Map Method.       Two- and Three-Variable Map.         Four-Variable Map.       Four-Variable Map.         Product of Sums Simplification.       Don't-Care Conditions.         (8)       NAND and NOR Implementation.       Lab 2         The Tabulation Method.       Simplification of Boolean       Functions using Tabulation         Method.       Simplification of Boolean       Functions using Tabulation         (9)       Analysis and Synthesis of Combinational Circuits:       Tutorial 3	(4)	Boolean Algebra and Logic Gates:	Lab 1
Basic Theorems.         Boolean Functions.         (5)       Standard Forms: Minterm and Maxterm.         Simplification of Boolean Functions using         SOP and POS.         (6)       Logic Operations: NAND, NOR,         Exclusive-OR and Equivalence.         Integrated Circuits         (7)       Gate-Level Minimization:         First Exam       The Map Method.         Two- and Three-Variable Map.         Four-Variable Map.         Product of Sums Simplification.         Don't-Care Conditions.         (8)       NAND and NOR Implementation.         The Tabulation Method.         Simplification of Boolean         Functions using Tabulation         Method.         (9)       Analysis and Synthesis of Combinational         Circuits:	(-)	Basic Definition	
Boolean Functions.(5)Standard Forms: Minterm and Maxterm. Simplification of Boolean Functions using SOP and POS.(6)Logic Operations: NAND, NOR, Exclusive-OR and Equivalence. Integrated Circuits(7)Gate-Level Minimization: The Map Method. Two- and Three-Variable Map. Four-Variable Map. Product of Sums Simplification. Don't-Care Conditions.(8)NAND and NOR Implementation. The Tabulation Method. Simplification of Boolean Functions using Tabulation Method.(9)Analysis and Synthesis of Combinational Circuits:		Basic Theorems.	
(5)Standard Forms: Minterm and Maxterm. Simplification of Boolean Functions using SOP and POS.(6)Logic Operations: NAND, NOR, Exclusive-OR and Equivalence. Integrated CircuitsTutorial 2(7)Gate-Level Minimization: The Map Method. Two- and Three-Variable Map. Four-Variable Map. Product of Sums Simplification. Don't-Care Conditions.Lab 2(8)NAND and NOR Implementation. Functions using TabulationLab 2(9)Analysis and Synthesis of Combinational Circuits:Tutorial 3		Boolean Functions.	
Simplification of Boolean Functions using SOP and POS.Tutorial 2(6)Logic Operations: NAND, NOR, Exclusive-OR and Equivalence. Integrated CircuitsTutorial 2(7)Gate-Level Minimization: The Map Method. Two- and Three-Variable Map. Four-Variable Map. Product of Sums Simplification. Don't-Care Conditions.Lab 2(8)NAND and NOR Implementation. Functions using Tabulation Method.Lab 2(9)Analysis and Synthesis of Combinational Circuits: Conclusion of CircuitsTutorial 3	(5)	Standard Forms: Minterm and Maxterm.	
SOP and POS.(6)Logic Operations: NAND, NOR, Exclusive-OR and Equivalence. Integrated CircuitsTutorial 2(7)Gate-Level Minimization: The Map Method. Two- and Three-Variable Map. Four-Variable Map. Product of Sums Simplification. Don't-Care Conditions.Table Map. Lab 2(8)NAND and NOR Implementation. The Tabulation Method. Simplification of Boolean Functions using Tabulation Method.Lab 2(9)Analysis and Synthesis of Combinational Circuits:Tutorial 3		Simplification of Boolean Functions using	
(6)Logic Operations: NAND, NOR, Exclusive-OR and Equivalence. Integrated CircuitsTutorial 2(7)Gate-Level Minimization: The Map Method. Two- and Three-Variable Map. Four-Variable Map. Product of Sums Simplification. Don't-Care Conditions.Tutorial 2(8)NAND and NOR Implementation. The Tabulation Method. Simplification of Boolean Functions using Tabulation Method.Lab 2(9)Analysis and Synthesis of Combinational Circuits: Circuits:Tutorial 3		SOP and POS.	
Exclusive-OR and Equivalence. Integrated Circuits(7)Gate-Level Minimization: The Map Method. Two- and Three-Variable Map. Four-Variable Map. Product of Sums Simplification. Don't-Care Conditions.(8)NAND and NOR Implementation. The Tabulation Method. Simplification of Boolean Functions using Tabulation Method.Lab 2(9)Analysis and Synthesis of Combinational Circuits: On the introduction of Combinational Circuits:Tutorial 3	(6)	Logic Operations: NAND, NOR,	Tutorial 2
Integrated Circuits(7)Gate-Level Minimization:First ExamThe Map Method.Two- and Three-Variable Map.Four-Variable Map.Product of Sums Simplification.Don't-Care Conditions.(8)NAND and NOR Implementation.The Tabulation Method.Simplification of BooleanFunctions using TabulationMethod.(9)Analysis and Synthesis of Combinational Circuits:Conduction of Conductional		Exclusive-OR and Equivalence.	
<ul> <li>(7) Gate-Level Minimization: The Map Method. Two- and Three-Variable Map. Four-Variable Map. Product of Sums Simplification. Don't-Care Conditions.</li> <li>(8) NAND and NOR Implementation. The Tabulation Method. Simplification of Boolean Functions using Tabulation Method.</li> <li>(9) Analysis and Synthesis of Combinational Circuits: Circuits: Circuits:</li> </ul>		Integrated Circuits	
First ExamThe Map Method. Two- and Three-Variable Map. Four-Variable Map. Product of Sums Simplification. Don't-Care Conditions.Lab 2(8)NAND and NOR Implementation. The Tabulation Method. Simplification of Boolean Functions using Tabulation Method.Lab 2(9)Analysis and Synthesis of Combinational Circuits: Don bit stimul CircuitsTutorial 3	(7)	Gate-Level Minimization:	
Two- and Three-Variable Map. Four-Variable Map. Product of Sums Simplification. Don't-Care Conditions.Lab 2(8)NAND and NOR Implementation. The Tabulation Method. Simplification of Boolean Functions using Tabulation Method.Lab 2(9)Analysis and Synthesis of Combinational Circuits: Circuits:Tutorial 3	First Exam	The Map Method.	
Four-Variable Map. Product of Sums Simplification. Don't-Care Conditions.Lab 2(8)NAND and NOR Implementation. The Tabulation Method. Simplification of Boolean Functions using Tabulation Method.Lab 2(9)Analysis and Synthesis of Combinational Circuits: Circuits:Tutorial 3		Two- and Three-Variable Map.	
Product of Sums Simplification. Don't-Care Conditions.Lab 2(8)NAND and NOR Implementation. The Tabulation Method. Simplification of Boolean Functions using Tabulation Method.Lab 2(9)Analysis and Synthesis of Combinational Circuits: Circuits:Tutorial 3		Four-Variable Map.	
Don't-Care Conditions.(8)NAND and NOR Implementation. The Tabulation Method. Simplification of Boolean Functions using Tabulation Method.Lab 2(9)Analysis and Synthesis of Combinational Circuits: Circuits:Tutorial 3		Product of Sums Simplification.	
<ul> <li>(8) NAND and NOR Implementation. The Tabulation Method. Simplification of Boolean Functions using Tabulation Method.</li> <li>(9) Analysis and Synthesis of Combinational Circuits:</li> </ul>		Don't-Care Conditions.	
The Tabulation Method.         Simplification of Boolean         Functions using Tabulation         Method.         (9)         Analysis and Synthesis of Combinational         Circuits:         Output	(8)	NAND and NOR Implementation.	Lab 2
<ul> <li>Simplification of Boolean Functions using Tabulation Method.</li> <li>(9) Analysis and Synthesis of Combinational Circuits:</li> </ul>		The Tabulation Method.	
Functions using Tabulation       Method.       (9)     Analysis and Synthesis of Combinational Circuits:		Simplification of Boolean	
(9) Analysis and Synthesis of Combinational Tutorial 3 Circuits:		Functions using Tabulation	
(9) Analysis and Synthesis of Combinational Tutorial 3 Circuits:		Method.	
Circuits:	(9)	Analysis and Synthesis of Combinational	Tutorial 3
		Circuits:	
Combinational Circuits.		Combinational Circuits.	
Analysis and Design Procedure.	(10)	Analysis and Design Procedure.	
(10) Binary Adders-Subtractor.	(10)	Binary Adders-Subtractor.	
Decoders and Multiplexers.	(11)	Decoders and Multiplexers.	
(11) Analysis and Synthesis of Sequential Second Exem	(11) Second Exem	Circuita:	
Second Exam Circuits.	Second Exam	Sequential Circuita	
Latches		Latches	
Elin-Flops: RS D IK and T		Flin-Flons: RS D IK and T	
(12) Analysis of Clocked Sequential Circuits	(12)	Analysis of Clocked Sequential Circuits	
Design Procedure	(12)	Design Procedure	
(13) Registers and Counters: Tutorial 4	(13)	Registers and Counters:	Tutorial 4
Registers		Registers	

	Shift Registers.	
(14)	Synchronous Counters.	Lab 3
	Ripple Counters.	
(15)	Sequential Circuits with Programmable	
Specimen	Logic Devices:	
examination	Introduction.	
(Optional)	Random-Access Memory.	
	Memory Decoding.	
	Read-Only Memory.	
	Programmable Logic Array.	
(16)	Review	
Final		
Examination		

## **Expected Workload:**

On average students need to spend 2 hours of study and preparation for each 50-minute lecture/tutorial.

#### **Attendance Policy:**

Absence from lectures and/or tutorials shall not exceed 15%. Students who exceed the 15% limit without a medical or emergency excuse acceptable to and approved by the Dean of the relevant college/faculty shall not be allowed to take the final examination and shall receive a mark of zero for the course. If the excuse is approved by the Dean, the student shall be considered to have withdrawn from the course.

#### **Module References**

Students will be expected to give the same attention to these references as given to the Module textbook(s)

- 1. <u>Morris Mano, Charles R. Kime, Logic and computer design fundamentals</u>, Pearson Prentice Hall, 2004
- 2. <u>Basavaraj, B.,</u> Digital fundamentals, New Delhi: Vikas Publishing House, 1999.
- 3. Kandel Langholz, Digital Logic Design, Prentice Hall, 1988.
- 4. Rafiquzzaman & Chandra, Modern Computer Architecture, West Pub. Comp., 1988.