Marking Scheme

Exam Paper
BSc CE

Logic Circuits (630211)

Final Exam  First semester  Date: 20/01/2013

Section 1
Weighting 40% of the module total

Lecturer: Dr. Qadri Hamarsheh
Coordinator: Dr. Ali Al-Khawaldeh
Internal Examiner: Dr. Anis Nazer
Marking Scheme

Logic Circuits (630211)

The presented exam questions are organized to overcome course material through 6 questions. The all questions are compulsory requested to be answered.

Marking Assignments

Question 1 This question is attributed with 10 marks if answered properly; the answers are the following:

1) Convert $11001001_2$ (binary) to decimal.
   a) 201
   b) 201
   c) 210
   d) 20

2) Convert the binary number $1011010$ to hexadecimal.
   a) 5B
   b) 5A
   c) 5F
   d) 5C

3) 3428 is the decimal value for which of the following binary coded decimal (BCD) groupings?
   a) $110100001101010$
   b) $11010000101000$
   c) $11010001001000$
   d) $011010010000010$

4) \( W \oplus X = \)
   a) \((W + X)(\overline{W} + \overline{X})\)
   b) \((W + \overline{X})(\overline{W} + X)\)
   c) \((W + X)(\overline{W} + \overline{X})\)
   d) \(WX + \overline{W} \overline{X}\)

5) Which output expression might indicate a product-of-sums circuit construction?
   a) \( Y = \overline{A} \cdot \overline{B} = \overline{A} + \overline{B} \)
   b) \( Y = (\overline{A} + \overline{B}) \cdot (A + B) \)
   c) \( Y = \overline{A} \overline{B} + C \overline{D} \)
   d) \( Y = \overline{A} \cdot \overline{B} = \overline{A} + \overline{B} \)

6) The fast carry or look-ahead carry circuits found in most 4-bit parallel-adder circuits:
   a) add a 1 to complemented inputs
   b) increase ripple delay
   c) reduce propagation delay
   d) determine sign and magnitude

7) Most demultiplexers facilitate which of the following?
   a) multiple inputs, single output
   b) decimal to hexadecimal
   c) odd parity to even parity
   d) single input, multiple outputs

8) A basic S-R flip-flop can be constructed by cross-coupling which basic logic gates?
   a) XOR or XNOR gates
   b) NOR or NAND gates
   c) AND or OR gates
   d) AND or NOR gates

9) For a D flip-flop, the next state is always equal to the D input.
   a) True
   b) False

10) A JK flip-flop is presently in the RESET state and must go to the SET state on the next clock pulse. J must be 1 and K must be X (don’t care).
    a) True
    b) False

Question 2 This question is attributed with 7 marks if answered properly; the answers are the following:

Question 2.1.a

Solution

\[ F = (AB)(\overline{CD}) + (B+C+A) + (BD\overline{A}) \]

(1 mark)

Question 2.1.b

Solution

\[
 f = \sum_{A,B,C,D} (1, 3, 8, 9, 12, 14, 15) = \prod_{A,B,C,D} (0, 2, 4, 5, 6, 7, 10, 11, 13) \\
 = (A+B+C+D)(A+B+C+D)(A+B+C+D) \\
     (A+B+C+D)(A+B+C+D)(A+B+C+D) \\
     (A+B+C+D)(A+B+C+D)(A+B+C+D) \\
     (A+B+C+D)(A+B+C+D)(A+B+C+D) \\
\]

(3 marks)
**Question 2.2**

Solution

\[
\begin{array}{c|c|c|c}
\text{\begin{tabular}{c c} \text{00} \end{tabular}} & \text{\begin{tabular}{c c} \text{01} \end{tabular}} & \text{\begin{tabular}{c c} \text{11} \end{tabular}} & \text{\begin{tabular}{c c} \text{10} \end{tabular}} \\
\hline
\text{0} & \text{0} & \text{1} & \text{1} \\
\text{1} & \text{0} & \text{0} & \text{X} \\
\text{1} & \text{X} & \text{1} & \text{0} \\
\end{array}
\]

\[f = AB + BC + BD + AB\overline{D}\]

**Question 3** This question is attributed with 6 marks if answered properly; the answers are the following:

**Question 3.a**

Solution

Implementation of Full Adder with two Half Adders and an OR gate

**Question 3.b**

Solution

Implementation of Full Adder with two Half Adders and an OR gate
Question 4 This question is attributed with 7 marks if answered properly; the answers are the following:

Question 4.a
The truth table for 3 bit Gray Code to binary conversion is as shown:

<table>
<thead>
<tr>
<th>Gray Code</th>
<th>Binary Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>$G_2$</td>
<td>$G_1$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Circuit Implementation

K-Maps:

$B_1 = G_2$

$B_1 = G_2 G_1 + G_2 G_1 = G_2 \oplus G_1$

$B_1 = G_2 G_1 + G_2 G_1 = G_2 \oplus G_1$

$B_1 = G_2 G_1 + G_2 G_1 = G_2 \oplus G_1$

$B_1 = G_2 G_1 + G_2 G_1 = G_2 \oplus G_1$

(3 marks)

Question 4.b
Truth table of half adder is as shown:

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A$</td>
<td>$B$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Circuit Implementation is as shown:

(2 marks)

(0.5 mark)

(1.5 marks)
**Question 5** This question is attributed with 4 marks if answered properly; the answers are the following:

**Excitation equations:** (0.5 mark)

\[
D_1 = C_{nt} \oplus Q_1 = \overline{C_{nt}} \cdot Q_1 + C_{nt} \cdot \overline{Q_1}
\]

\[
D_2 = \overline{C_{nt}} \cdot Q_2 + C_{nt} \cdot \overline{Q_2} \cdot Q_1 + C_{nt} Q_2 \overline{Q_1}
\]

**Next-state equations:**

\[
Q_1(\text{next}) = D_1 = C_{nt} \oplus Q_1 = \overline{C_{nt}} \cdot Q_1 + C_{nt} \cdot \overline{Q_1}
\]

\[
Q_2(\text{next}) = D_2 = \overline{C_{nt}} \cdot Q_2 + C_{nt} \cdot \overline{Q_2} \cdot Q_1 + C_{nt} Q_2 \overline{Q_1}
\]

**Output equation:** (0.5 mark)

\[
Y = Q_2 \cdot Q_1
\]

**Next-state and output table:** (1.5 marks)

<table>
<thead>
<tr>
<th>Present State</th>
<th>Input</th>
<th>Next State</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q₂</td>
<td>Q₁</td>
<td>Cnt</td>
<td>Q₂</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<tr>
<td>0</td>
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<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**State diagram:** (1.5 marks)
Question 6 This question is attributed with 6 marks if answered properly; the answers are the following: 

Step 1: Construct the state diagram as below: 

Step 2: Construct the state table as below:

<table>
<thead>
<tr>
<th>Present State</th>
<th>Next State</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_2$ $Q_1$ $Q_0$</td>
<td>$Q_2$ $Q_1$ $Q_0$</td>
</tr>
<tr>
<td>1 1 1</td>
<td>1 1 0</td>
</tr>
<tr>
<td>1 1 0</td>
<td>1 0 1</td>
</tr>
<tr>
<td>1 0 1</td>
<td>1 0 0</td>
</tr>
<tr>
<td>1 0 0</td>
<td>0 1 1</td>
</tr>
<tr>
<td>0 1 1</td>
<td>0 1 0</td>
</tr>
<tr>
<td>0 1 0</td>
<td>0 0 1</td>
</tr>
<tr>
<td>0 0 1</td>
<td>1 0 0</td>
</tr>
<tr>
<td>0 0 0</td>
<td>0 1 1</td>
</tr>
</tbody>
</table>

Step 3: Construct JK excitation table:

<table>
<thead>
<tr>
<th>Present State $Q(t)$</th>
<th>Next State $Q(t+1)$</th>
<th>$J$</th>
<th>$K$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>0 0</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>0 1</td>
<td>1 1</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>1 0</td>
<td>X 1</td>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1 1</td>
<td>X 0</td>
<td>X</td>
<td>1</td>
</tr>
</tbody>
</table>

Step 4: State table with corresponding excitation table:

<table>
<thead>
<tr>
<th>Present State $Q(t)$</th>
<th>Next State $Q(t+1)$</th>
<th>$J$</th>
<th>$K$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>0 0</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>0 1</td>
<td>X 0</td>
<td>X</td>
<td>1</td>
</tr>
<tr>
<td>1 0</td>
<td>X 1</td>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1 1</td>
<td>X 0</td>
<td>X</td>
<td>1</td>
</tr>
<tr>
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<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0 1</td>
<td>0 0</td>
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<td>X</td>
</tr>
<tr>
<td>1 0</td>
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<td>1</td>
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<td>0 0</td>
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<td>0</td>
<td>0</td>
</tr>
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<td>0 0</td>
<td>0</td>
<td>X</td>
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<tr>
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<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1 1</td>
<td>1 0</td>
<td>1</td>
<td>X</td>
</tr>
</tbody>
</table>

Step 5: Build Karnaugh Map for each JK inputs:

Step 6: Draw the complete design as below:

3-bit synchronous down counter with JK flip-flop circuit