Marking Scheme

Exam Paper
BSc CE

Logic Circuits (630211)

Final Exam Second Semester Date: 06/08/2016
Section 1
Weighting 40% of the module total

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The presented exam questions are organized to overcome course material through 5 questions. The all questions are compulsory requested to be answered.

Marking Assignments

**Question 1** This question is attributed with **13 marks** if answered properly; the answers are the following:

1) Convert hexadecimal **C0B** to binary.
   a) 110000001100  
   b) 110100001011  
   c) 110000001001  
   d) 110000001011

2) Using Boolean algebra theorem gives $x(x + y)$ equal to
   a) $\bar{x}$  
   b) 1  
   c) 0  
   d) $x$

3) Refer to the following figure, If $S_1=1$ and $S_2=0$ what will be the logic state at the output $X$?

   a) $X = A$  
   b) $X = B$  
   c) $X = C$  
   d) $X = D$

4) The minterms in a karnaugh map are marked with a
   a) $y$  
   b) $x$  
   c) 0  
   d) 1

5) A **6x64** line decoder can be built using:
   a) six 2x4 line decoders only  
   b) nine 2x4 line decoders only  
   c) seven 3x8 line decoders only  
   d) nine 3x8 line decoders only

6) Decoder with enable input can be used as:
   a) XOR  
   b) Demultiplexer  
   c) Multiplexer  
   d) Encoder

7) The Boolean function realized by the logic circuit shown is

   a) $F = \Sigma m (0, 1, 3, 5, 9, 10, 14)$  
   b) $F = \Sigma m (2, 3, 5, 7, 8, 12, 13)$  
   c) $F = \Sigma m (1, 2, 4, 5, 11, 14, 15)$  
   d) $F = \Sigma m (2, 3, 5, 7, 8, 9, 12)$

8) A sequential circuit with two **JK** flip-flops $A$ and $B$, and one input $X$ is specified by the following input equations:

   $J_A = B X'$  
   $K_A = A' X'$  
   $J_B = A' X'$  
   $K_B = B X' + A' X$

   What are the next states of the flip-flops $A$ and $B$ if the present state of the flip-flops $A$, $B$ and the input $X$ equals, **001, 101** respectively:

   a) 01, 10  
   b) 00, 10  
   c) 01, 01  
   d) 01, 11

9) What is the function of the following circuit?

   a) A four-bit memory register.  
   b) A four-bit synchronous counter.  
   c) A four-bit shift register.  
   d) None of the above
10) In a **synchronous** counter, each state is clocked by the same pulse.
   a) True  
   b) False

11) Fastest operating shift register is:
   a) Serial In - Serial Out
   b) Serial In - Parallel Out
   c) Parallel In - Serial Out
   d) Parallel In - Parallel Out

12) Two **4-bit** shift registers A and B with serial input (SI) and serial output (SO), the initial content of register A and B, 1100, 1110 respectively. The SO of register A is connected to the SI of register B. The register A shifted eight times with the serial input being 10111011. What are the content of the register A and B after the **fifth shift** (T5)?
   a) 1110, 0111 respectively  
   b) 1011, 1101 respectively  
   c) 1110, 1110 respectively  
   d) 1001, 1110 respectively

13) Number of clock pulses, which **5-bit ring** counter needs to reach 00010 state are (initial state of the counter 10000):
   a) 3  
   b) 5  
   c) 7  
   d) 9

**Question 2** This question is attributed with **9 marks** if answered properly; the answers are the following:

a) 

   **Solution**

   \[
   F = AB'CD' + A'B'CD + AB'C'D + A'BC'D
   = AB'(CD' + C'D) + A'B(C'D + C'D)
   = (AB' + A'B)(CD' + C'D)
   = (A \oplus B)(C \oplus D)
   \]

b) 

   **Solution**

   ![K-map for Y]

   \[ Y = CD + C'D' \]

c) 

   **Solution**

   ![Truth table for f(w, x, y, z) = wx + xz + y]

   \[ f(w, x, y, z) = wx + xz + y \]
Question 3 This question is attributed with 5 marks if answered properly; the answers are the following:

a) 

b) 

(3 marks)
Question 4 This question is attributed with 6 marks if answered properly; the answers are the following:

Solution

Question 5 This question is attributed with 7 marks if answered properly; the answers are the following:

<table>
<thead>
<tr>
<th>Input</th>
<th>Current state $x$</th>
<th>Current state $q_1$</th>
<th>Current state $q_2$</th>
<th>Next state $Q_1$</th>
<th>Next state $Q_2$</th>
<th>$S_1$</th>
<th>$R_1$</th>
<th>$S_2$</th>
<th>$R_2$</th>
<th>Output $y$</th>
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$S_1 = (xq_1)q_1' + xq_1'q_2 = ((xq_2) + xq_2)q_1'$

$R_1 = x'q_1q_1' + xq_1q_2 = (xq_2)' + xq_2q_1$'

$S_2 = q_2'$

$R_2 = q_2$