Information for candidates
1. This exam paper contains 5 questions totaling 20 marks
2. The marks for parts of question are shown in round brackets.

Advices to candidates
1. You should attempt all sub questions.
2. You should write your answers clearly.

Question 1  Multiple Choice (5 marks)
Identify the choice that best completes the statement or answers the question.

1. Karnaugh map technique provides a systematic method for simplifying -----------:
   a) Multiplexers   b) Boolean expressions
   c) Logic gates    d) None of these

2. To add or subtract the following two binary numbers 10001101 and 10001110, we need Adder/Subtractor contains at least:
   a) 8 half adders and 8 XOR gates.
   b) 16 half adders and 16 XOR gates.
   c) 8 full adders and 8 XOR gates.
   d) 16 full adders and 16 XOR gates.

3. In half adder, the XOR gate is used to execute the -----------:
   a) Sum   b) Carry
   c) Remainder   d) None of these

4. To implement binary full adder using decoders we need:
   a) 3-to-8 decoder with two OR logic gates
   b) 3-to-8 decoder with one OR logic gate
   c) 3-to-8 decoder with one AND logic gates
   d) None of above

5. A flip-flop that operates in step with the clock is said to operate -----------:
   a) asynchronously   b) synchronously
**Question 2** For the following Boolean expression:

$$f (A, B, C, D) = \overline{A} \overline{B} + CD + AC + B\overline{C}D + \overline{A}B\overline{C}\overline{D}$$

(a) List the **Prime Implicants** of $f$ (3 marks)
(b) List the **Essential Prime Implicants** of $f$ (1 mark)
(c) Write the **minimum SOP** for $f$ (2 marks)

**Solution**
Question 3

(4 marks)

Design A $4 \times 4$ binary multiplier circuit.
**Question 4** Implement a 3-variables *Majority function* using *4x1 multiplexer*. (3 marks)

**Solution**

**Question 5**
For the RS flip-flop with positive edge clock, draw the output $Q$ of the following timing diagram:

*GOOD LUCK*