Information for candidates
1. This exam paper contains 4 questions totaling 20 marks.
2. The marks for parts of question are shown in round brackets.

Advises to candidates
1. You should attempt all sub questions.
2. You should write your answers clearly.

**Question 1**
Multiple Choice (5 marks)
Identify the choice that best completes the statement or answers the question.

1) When grouping cells within a K-map, the cells must be combined in groups of ________s
   a) 2  
   b) 4  
   c) 3  
   d) 2^n

2) The Boolean function $F$ with don't-care conditions are represented in the K-map for four-variables as shown below, the simplification of the function $F$ in sum-of-products form is:

   a) $\overline{A}D + \overline{A}B + BD + \overline{C}D$
   b) $\overline{A}D + \overline{A}B + \overline{C}D + A\overline{B}\overline{C}D$
   c) $\overline{A}D + BD + \overline{C}D$
   d) $\overline{A}BD + \overline{A}B + BD + A\overline{B}\overline{C}D$

3) What are the two types of basic adder circuits?
   a) half adder and parallel adder
   b) half adder and full adder
   c) asynchronous and synchronous
   d) one's complement and two's complement

4) An 8-to-1 multiplexer has inputs $A$, $B$ and $C$ connected to the selection inputs $S_2$, $S_1$ and $S_0$, respectively. The data inputs $I_0$ through $I_7$ are as follows:
   $I_1 = I_2 = 0; I_3 = I_5 = I_7 = 1; I_0 = I_4 = \overline{D}$ and $I_6 = D$
   The Boolean function that the multiplexer implements is:
   a) $F = \Sigma m (0, 6, 7, 8, 10, 11, 13, 14, 15)$
   b) $F = \Sigma m (1, 2, 3, 4, 5, 9, 12)$
   c) $F = \Sigma m (0, 6, 7, 8, 9, 11, 13, 14, 15)$
   d) $F = \Sigma m (0, 6, 7, 9, 11, 14, 15)$

5) How many select lines are there for a 1 to 32 Demultiplexer?
   a) 4  
   b) 5  
   c) 6  
   d) 8
2.1) Draw the circuit of **Adder-Subtractor** which can add or subtract two digits each contain three bits. (6 marks)

### Solution

2.2) Consider the following **decoder**:

![Diagagram of a 2x4 decoder with inputs I0, I1 and outputs O0, O1, O2, O3, and Enable.]

a) Draw the **internal structure** of the decoder, including any inverters at the inputs. (2 marks)

### Solution
b) Build a **3x8 decoder** with **active low output** using the above decoder and an **inverter** only.  
(2 marks)

**Solution**

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**Question 3**  
(5 marks)  
Design **BCD to Excess-3** code converter using **decoder 4x16**.

**Solution**
Given the following truth table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

a) Use an 8:1 Multiplexer to generate (implement) $F$.

Solution:

b) Generate $F$ using a 4 to 1 Mux.

Solution:

GOOD LUCK