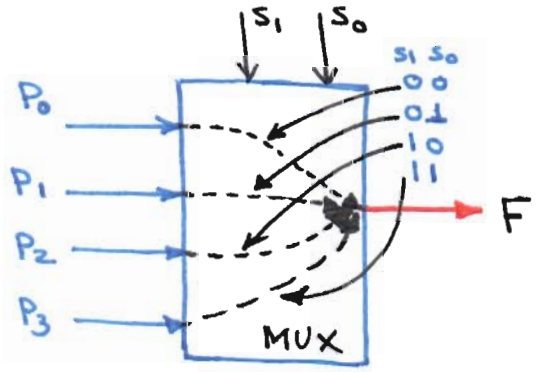
Multiplexers

- A multiplexers (MUX) is a combinational logic component that has several inputs and only one output. MUX directs one of the input to its output line by using a control bit word (selection line) to its select lines.

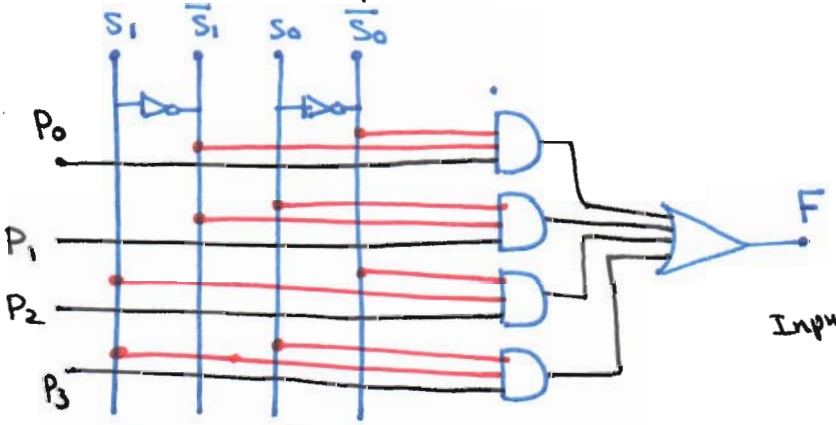
• 4-to-1 multiplexers

- S_1, S_0 - Select lines.
- P_0, P_2, P_3, P_1 - Input lines.
- F - single output line.

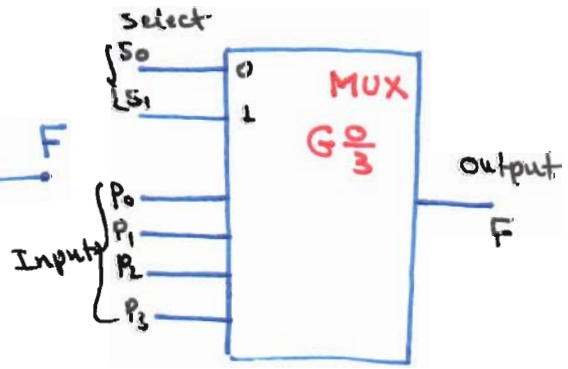


Select lines		output (F)
S_1	S_0	F
0	0	P_0
0	1	P_1
1	0	P_2
1	1	P_3

$$F = \overline{S_1}\,\overline{S_0} \cdot P_0 + \overline{S_1} S_0 P_1 + S_1 \overline{S_0} P_2 + S_1 S_0 P_3$$



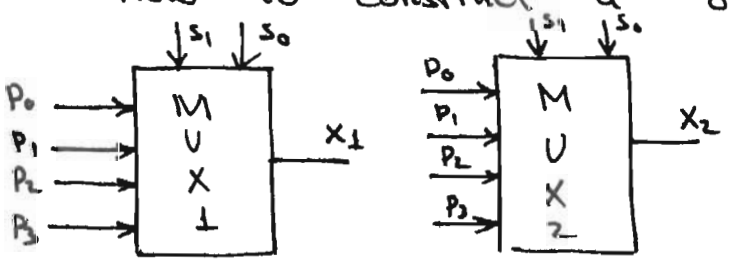
Internal logic circuit for 4-1 MUX



4:1 MUX module "digital element".

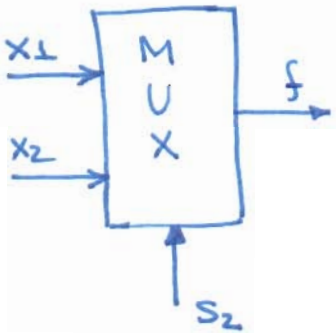
• Design of a 8:1 Multiplexer

How to construct a 8:1 MUX from two 4:1 MUX.



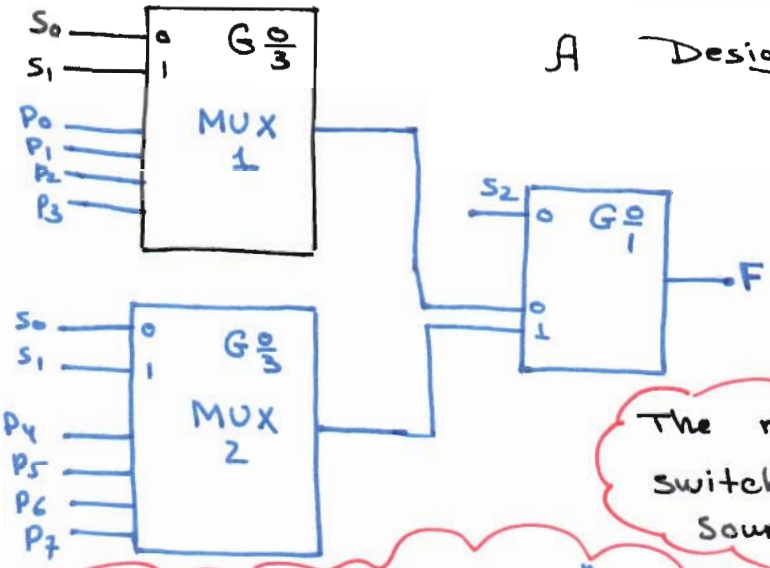
X_1 and X_2 are the two output lines of two 4:1 MUX.

$$X1 = \bar{S}_1 \bar{S}_0 P_0 + \bar{S}_1 S_0 P_1 + S_1 \bar{S}_0 P_2 + S_1 S_0 P_3$$
$$X2 = \bar{S}_1 \bar{S}_0 P_0 + \bar{S}_1 S_0 P_1 + S_1 \bar{S}_0 P_2 + S_1 S_0 P_3$$



$$f = \bar{S}_2 X_1 + S_2 X_2$$

The multiplexer sometime is called Data selector



A Design for a 8:1 MUX Network.

: n- select lines : S_0, S_1, S_2

$2^n : 1 \rightarrow$ MUX.

The multiplexer acts like an electronic switch that selects one from differenet sources.

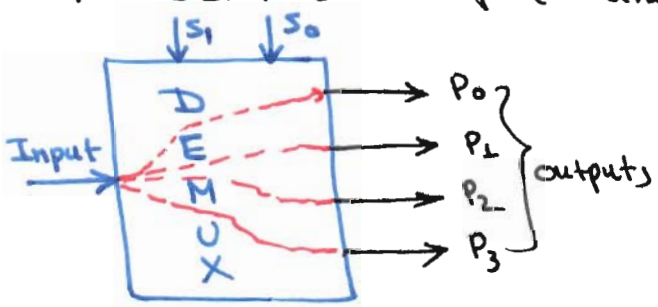
* Normally, there are 2^n input lines and n selection lines whose bit combinations determine which input is selected.

A multiplexer may have an enable input to control the operation of the unit.

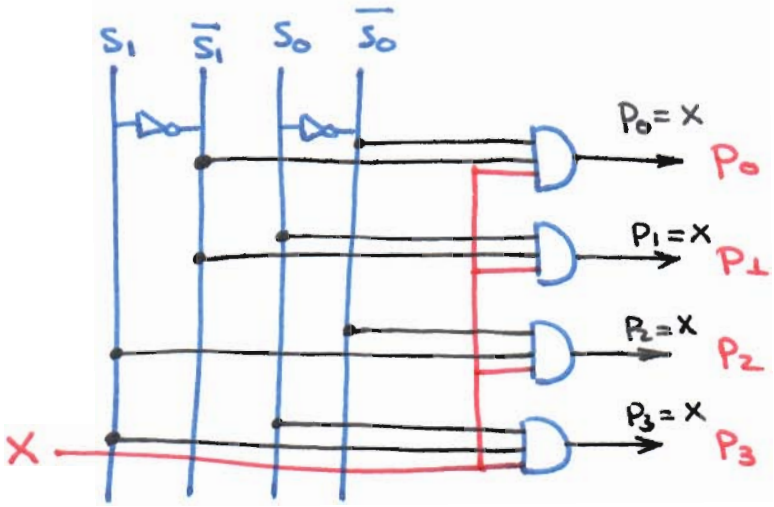
Demultiplexers.

The demultiplexer is a combinational logic circuit that performs the reverse operation of multiplexer.

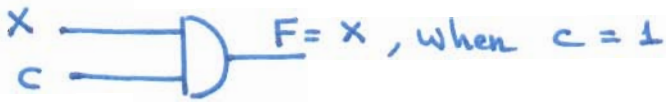
(Several output lines, one input line).

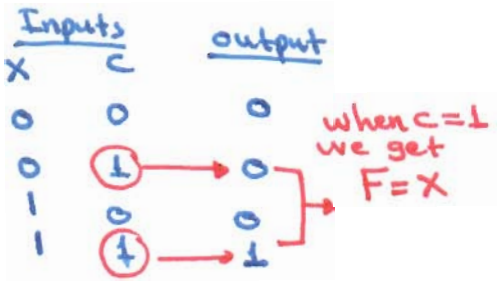


Internal logic circuit for 1:4 demultiplexer



Explain:





Two Select lines ⇒ four outputs

$\bar{S}_1 \bar{S}_0 = 0\,0 \Rightarrow P_0 = X$

$S_1 \bar{S}_0 = 0\,1 \Rightarrow P_1 = X$

$\bar{S}_1 S_0 = 1\,0 \Rightarrow P_2 = X$

$S_1 S_0 = 1\,1 \Rightarrow P_3 = X$

Encoders

An encoder is a digital circuit that performs the inverse operation of a decoder.

An encoder has 2^n (or fewer) input lines and n output lines.

Inputs								outputs		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	X	Y	Z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Truth table of an octal-to-Binary Encoder

The encoder can be implemented with OR gates whose inputs are determined directly from the truth table.

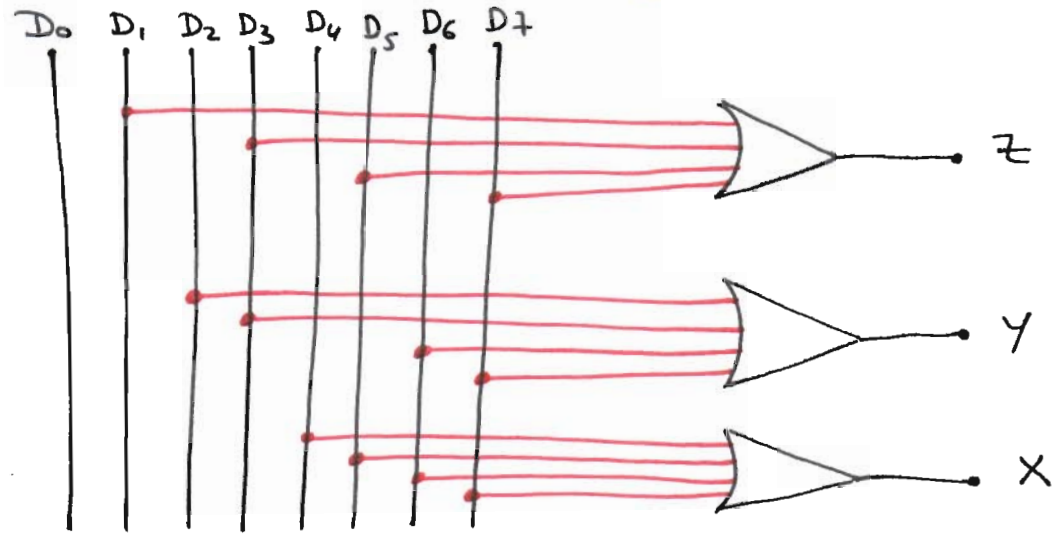
* output z is equal to 1 when the input digit is 1, 3, 5 or 7.

$$Z = D_1 + D_3 + D_5 + D_7$$

$$Y = D_2 + D_3 + D_6 + D_7$$

$$X = D_4 + D_5 + D_6 + D_7$$

We need three OR gates



End of Part 2