1. Analysis with D Flip-flop.

Example : Consider the following equation (input equation) for D flip-flop.

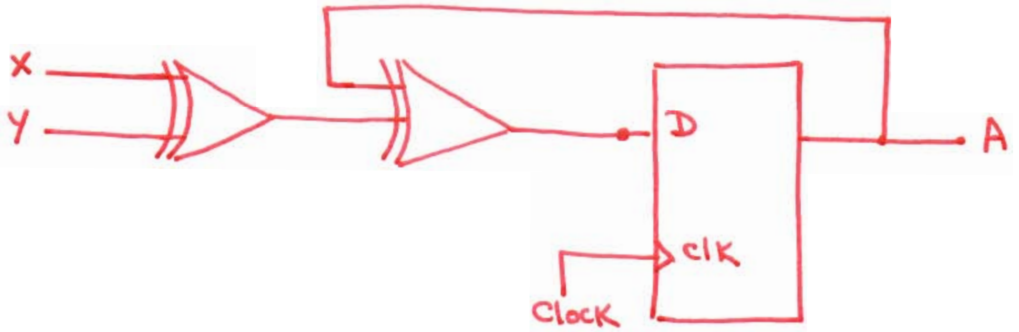
$$D_A = A \oplus x \oplus y$$

where ; DA - D flip-flop with output A.
x and y are the inputs to the circuit.

Do the following :
a- Draw the sequential Circuit
b- Construct the state table.
c- construct the state diagram.

Solution :
- No output equations are given.

a- The logic diagram is obtained from the input equation.

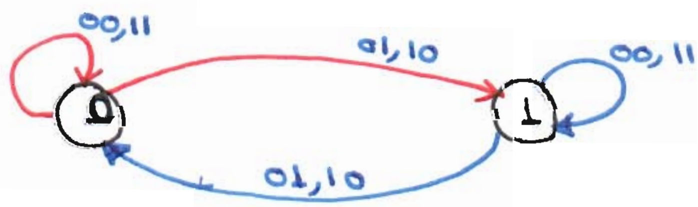


b- The state table has one column for the present state of flip-flop A, two columns for two inputs and one column for the next state.
The next state values are obtained from the state equation: $A(t+1) = A \oplus x \oplus y$

State table

Present state A	Inputs x	Inputs y	Next State A(t+1)
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

c-



* A slash on the directed line is not needed because No output from a combinational Circuit.

* Two inputs ⟶ four combinations
* one flip-flop ⟶ Two combination

2. Analysis with JK Flip-flops.

State table consists of: present state, inputs, next state and outputs.

The output section is determined from the output equation. The next state values are evaluated from the state equations.

* for D type: the equation is the same as the input equation.

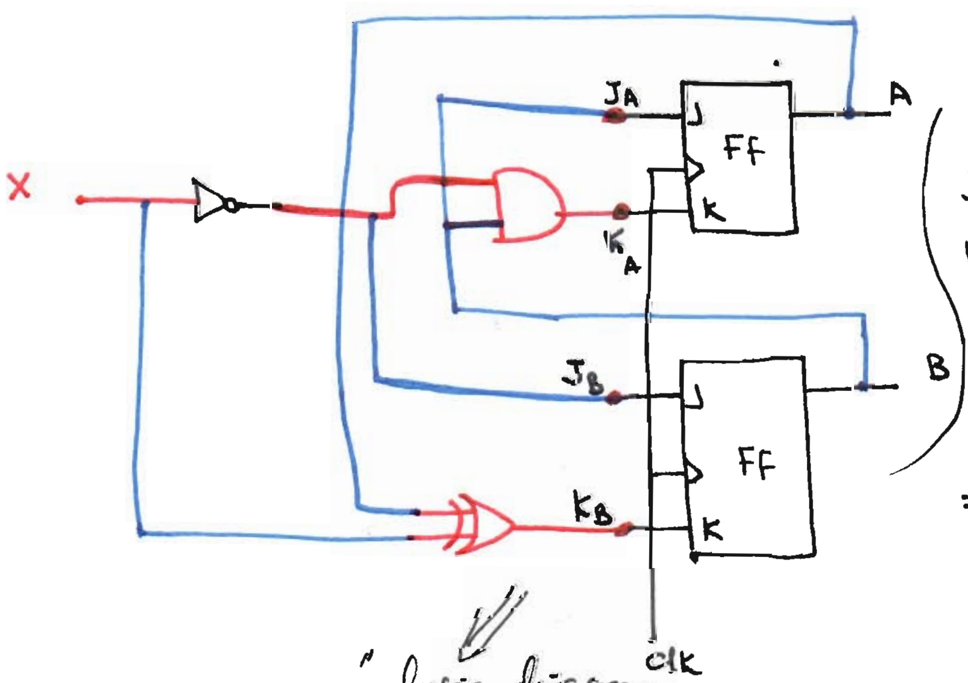
When a flip-flop other than the D type is used, such as JK or T, it is necessary to refer to the corresponding characteristics table or characteristic equation to obtain the next-state values.

The next-state values for JK or T or SR Types can be derived as follows:

1. Determine the input equations (for flip-flop)
2. list the binary values.
3. Use Characteristics table to determine the next-state values.

example:

Consider the sequential circuit with two JK flip-flops A and B and one input x, the circuit has no outputs. (the state table does not need output column)



"logic diagram"

Input Equations:

$J_A = B$
$K_A = B \cdot \overline{X}$
} flip-flop A

$J_B = \overline{X}$
$K_B = A \oplus X$
$= A\overline{X} + \overline{A}B$
} flip-flop B

[illegible]

Present state A	Present state B	Input X	Next state A	Next state B	Flip-Flop Inputs J_A	K_A	J_B	K_B
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	1	1	0	0	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	0

No change

Complement

③ ② ①

State table for JK Flip-flops

* The binary values listed under Flip-flop Inputs are not part of the ② state table.
* they are needed to calculate the next state value (step 2 of the procedure)

* The flip-flop Inputs values are obtained directly from the input equations.

* The next state of each flip-flop is evaluated from ① the corresponding j and K inputs and the characteristics table of the JK flip-flop.

② The next-state values can be obtained by evaluating the state equation from the characteristic equation:

Procedure:

1. Determine the flip-flop input equations.
2. Substitue the input equations into the flip-flop characteristics equation to obtain the state equations.
3. Use state equations to determine the next-state values in the state table.

1). $J_A = B \qquad K_A = B\overline{X}$

$J_B = \overline{X} \qquad K_B = \overline{A}X + A\overline{X} = A \oplus X$ } → input equations.

2) characteristics equations (substitue A or B ~~instead~~ instead of Q.

$$A(t+1) = J\overline{A} + \overline{K}A \rightarrow \text{(for A flip flop)}$$

$$B(t+1) = J\overline{B} + \overline{K}B \quad \text{(for B flip flop)}$$

→ Charactresrtcs equations for A and B flip flop

Substituting the values of J_A and K_A from the input equations, we obtain the state equations for A:

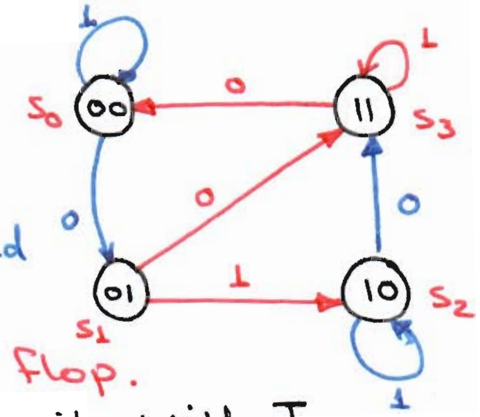
$$A(t+1) = B\bar{A} + \overline{(B\bar{X})} \cdot A = \bar{A}B + A\bar{B} + AX$$

and for the flip-flop B is:

$$B(t+1) = \bar{X}\bar{B} + \overline{(A \oplus X)} \cdot B = \bar{B}\bar{X} + ABX + \bar{A}B\bar{X}$$

3. Calculate the state table values from these equations.

The state diagram of the sequential circuit (Note: the circuit has no outputs, the directed lines marked with one binary number).



3. Analysis with T Flip-flop.

The analysis of a sequential circuit with T flip-flop follows the same procedure as for JK flip-flops.

The next-state values in the state table can be obtained by using either the characteristics table or characteristic equation

$$Q(t+1) = T \oplus Q = \bar{T}Q + T\bar{Q}$$

example: consider the sequential circuit, with two flip-flops A and B, one input x and one output y, and has the following input equations and output equation:

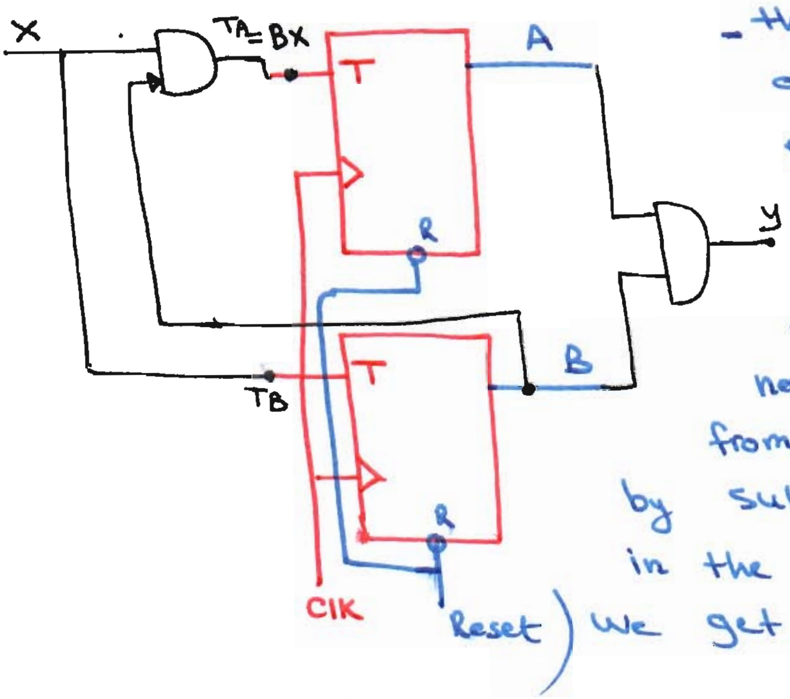
$$T_A = BX$$
$$T_B = X$$
$$y = AB.$$

Do the following:

1. Draw the logic diagram.
2. construct the state table.
3. construct the state diagram.

Solution:

1)



2) * the state table:

- the values of y are obtained from the output equation.

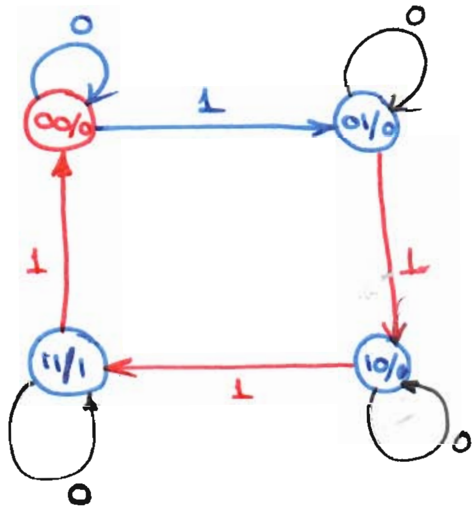
- the values for the next state can be derived from the state equations by substituting T_A and T_B in the characteristic equation, we get:

$$A(t+1) = \overline{(BX)}\,A + (BX)\cdot\bar{A} = A\bar{B} + A\bar{X} + \bar{A}BX$$

$$B(t+1) = X \oplus B.$$

Present state A	Present state B	Input X	Next state A	Next state B	output y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	1

State table



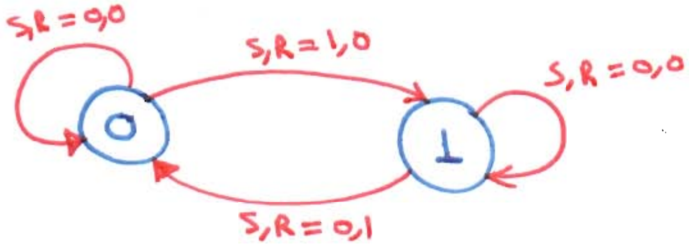
State diagram.

Notes: • X = 1 ⟶ the Circuit behaves as a binary counter with sequence of states 00, 01, 10, 11, and back to 00.

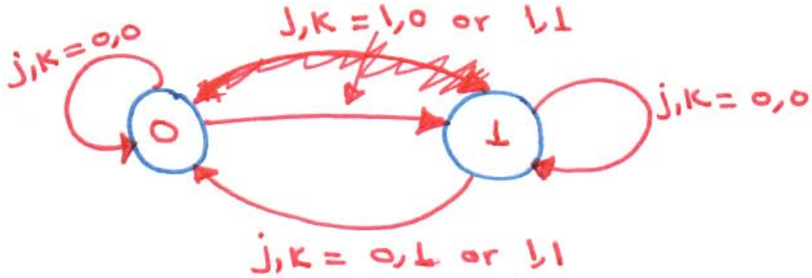
- When X = 0 ⟶ the circuit remains in the same state.
- output y is equal to 1, when the present state 11

Summary for state diagrams of Various Flip-Flops.

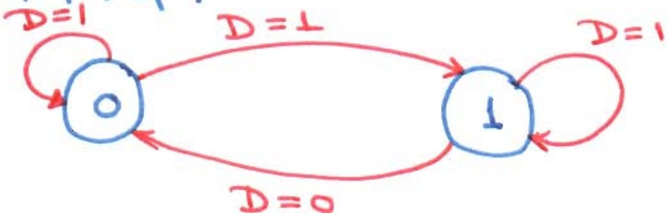
1. SR flip-flop :



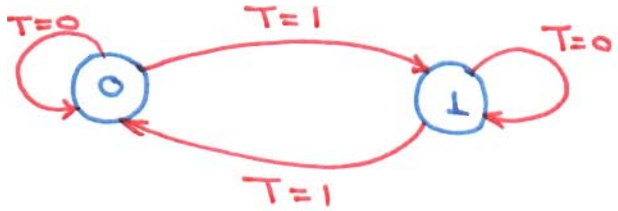
2. JK flip-flop :



3. D- flip-flop :

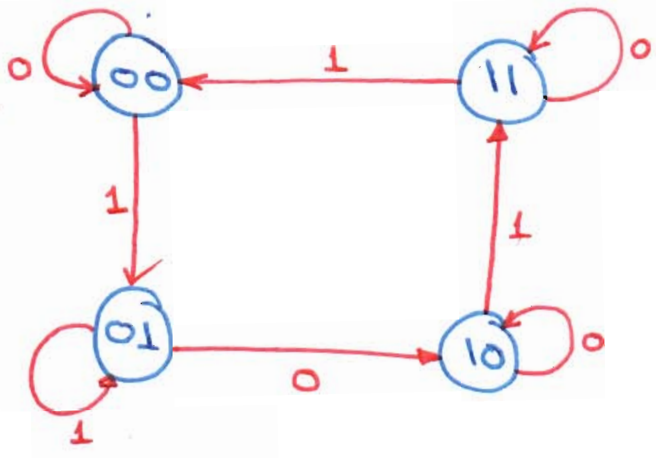


4. T flip-flop :



Example :

Design a synchronous sequential circuit whose state diagram is shown and the type of flip-flop to be use is j-K.



Solution :

1. from the state diagram, we get state table :

Present state		Next state			
		X=0		X=1	
Q_0	Q_1	Q_0	Q_1	Q_0	Q_1
0	0	0	0	0	1
0	1	1	0	0	1
1	0	1	0	1	1
1	1	1	1	0	0

table 1

* No output section for this circuit.

2. Construct the excitation table and the Combinational structure.

- Excitation table for jK flip-flop :

Q(t)	Q(t+1)	j	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

table 2

* from table 1 and table 2.

Excitation table of the circuit.

Present state Q_0	Present state Q_1	Next state Q_0	Next state Q_1	Input X	Flip-flop Inputs $J_0 K_0$	Flip-flop Inputs $J_1 K_1$
0	0	0	0	0	0 X	0 X
0	0	0	1	1	0 X	1 X
0	1	1	0	0	1 X	X 1
0	1	0	1	1	0 X	X 0
1	0	1	0	0	X 0	0 X
1	0	1	1	1	X 0	1 X
1	1	1	1	0	X 0	X 0
1	1	0	0	1	X 1	X 1

table 3.

from table 3: first row: we have a transition for flip-flop Q_0 from 0 in the present state to 0 in the next state. ⇒ the input of jK as in table must be $j = 0$ and $K = X$.

The output are j_0, K_0, j_1 and K_1, the inputs are Q_0, Q_1 and X.

* The information from the truth table is plotted on the Karnaugh maps:

Q_0Q_1 \ X	0	1
00	0	0
01	1	0
11	X	X
10	X	X

j_0 map

Q_0Q_1 \ X	0	1
00	X	X
01	X	X
11	0	1
10	0	0

K_0 map

Q_0Q_1 \ X	0	1
00	0	1
01	0	X
11	0	X
10	0	1

J_1 map

Q_0Q_1 \ X	0	1
00	X	X
01	1	0
11	0	1
10	X	X

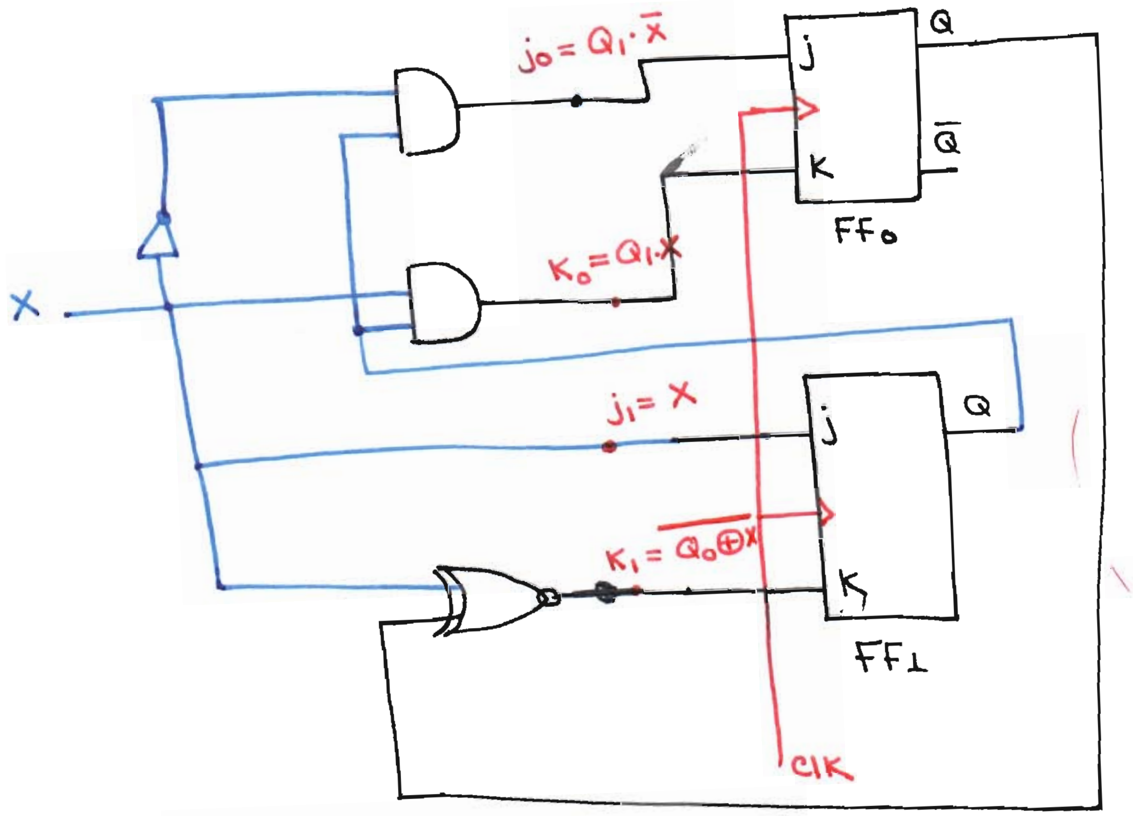
K_1 map

The flip-flop input functions are derived:

$$J_0 = Q_1 \cdot \overline{X} \qquad K_0 = Q_1 \cdot X$$

$$J_1 = X \qquad K_1 = \overline{Q_0} \cdot \overline{X} + Q_0 \cdot X = \overline{Q_0 \oplus X}$$

↙ exclusive NOR



Logic Diagram of the sequential Circuit.