Registers

1. Introduction
2. Types of registers.
3. Applications of registers.

1. Introduction :

shif registers are a type of sequential logic circuit, used mainly for storage.
They are a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop.

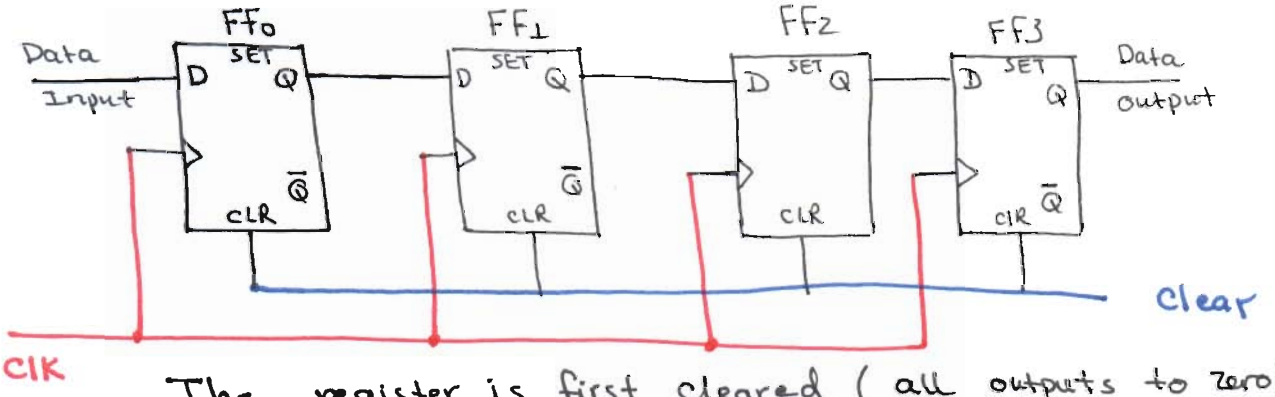
2. Types of registers :

the basic types of shif registers are

- Serial In - Serial out shift registers.
- Serial In - Parallel out shift registers.
- Parallel In - Serial out shift registers.
- Bidirectional shift registers.
- shift register counters.

① Serial In - Serial out shift registers:

A basic four-bit shift register can be constructed using D flip-flops.



- The register is first cleared (all outputs to zero)

Clear →

FF0	FF1	FF2	FF3
0	0	0	0

- The input data is then applied sequentially to the D input of the first flip-flop (FF0).
- During each clock pulse, one bit is transmitted from left to the right.

Assume the data word is 1001 ⇒
In order to get the data out of the register, ~~they~~ they must

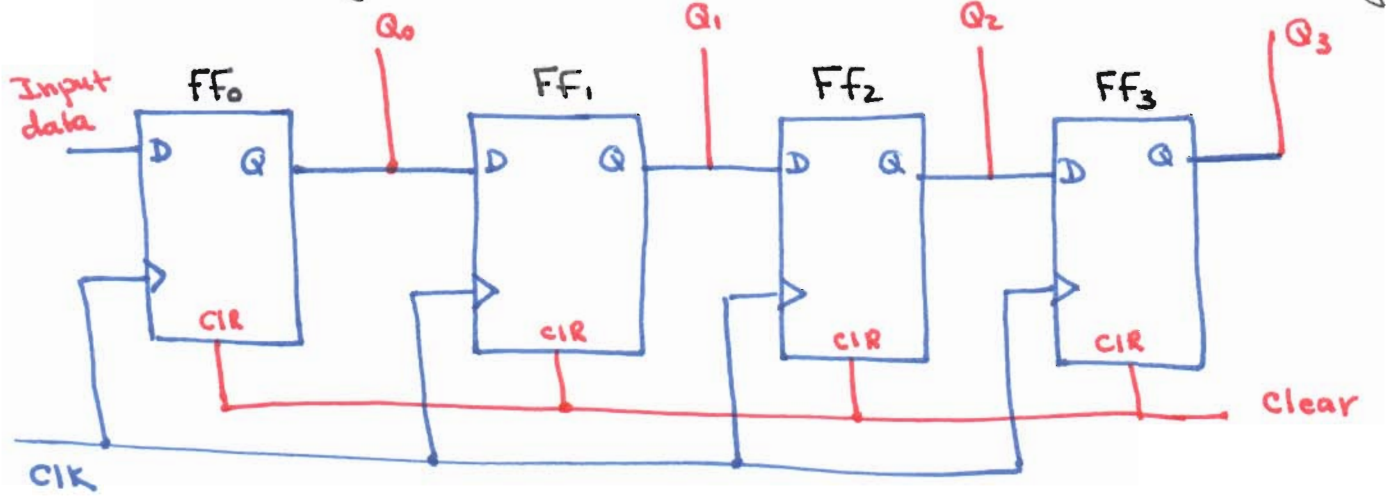
be shifted out serially.

FF0	FF1	FF2	FF3
1	0	0	1

2. Serial In - parallel out shift Registers.

in this Kind of registers: data bits are entered serially, and the difference is the way in which the data bits are taken out of the register.

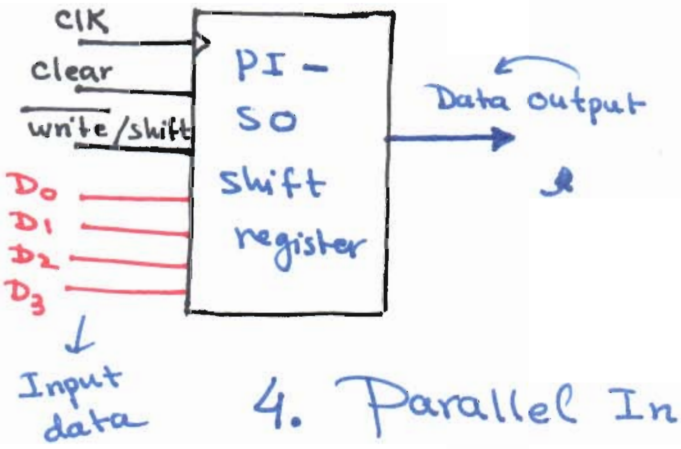
after storing the data, all bits are available simultaneously.



3. Parallel In - Serial out shif Registers.

* Logic Circuit → See textbook.

(the Circuit uses D flip-flops and NAND gates for entering data to the register.

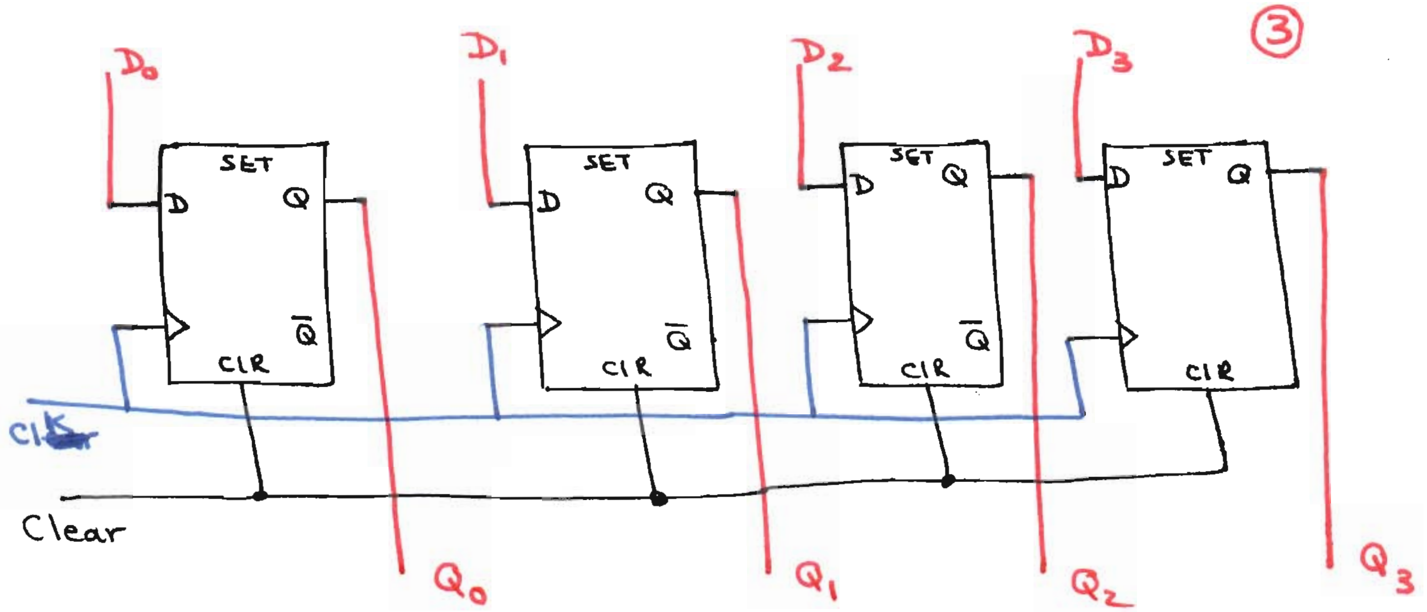


- D_0, D_1, D_2, D_3 are the parallel inputs.
- $\overline{write}$/ shift : mode control line : 0 → write the data
  : 1 → shifting mode.
  (right shift operation)

4. Parallel In - Parallel out shift registers.

all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits.

The D's are the ~~parralel~~ parallel inputs and the Q's are the parallel outputs.



PI – PO shift register structure.

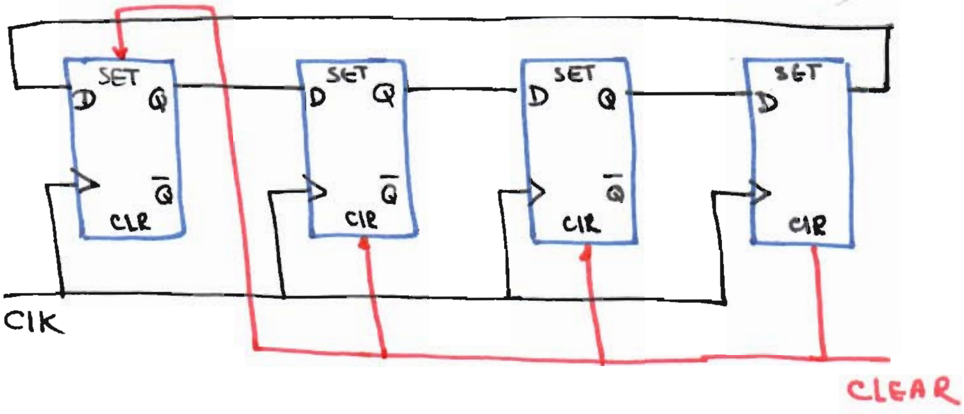
- **Shift Register Counters :**
  - Ring counter.
  - Johnson counter.

They are basically shift registers with the serial outputs connected back to the serial inputs in order to produce particular sequences.

- Ring Counters :

A ring counter is basically a circulating shift register in which the output of the most significant stage is fedback to the input of the least significant stage.
if the CLEAR signal is high : all the flip-flops except the first one FFo are reset to 0.
The count sequence has 4 states (from all 16 states)

Clock pulse	Q_3	Q_2	Q_1	Q_0
0	0	0	0	1
1	0	0	1	0
2	0	1	0	0
3	1	0	0	0

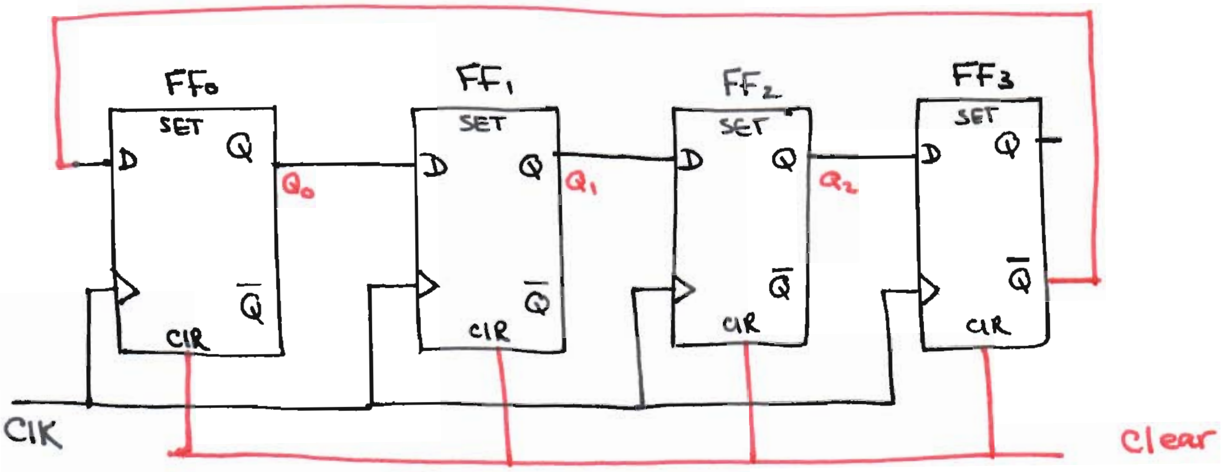


	FFo	FF1	FF2	FF3
Clear = 1	1	0	0	0

* disadvantage : only 4 states are used (inefficient).

* advantage : (over the binary counters) is that it is self-decoding (No extra decoding circuit is needed to determine the states).

• Johnson Counter



clock pulse	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	1
3	0	1	1	1
4	1	1	1	1
5	1	1	1	0
6	1	1	0	0
7	1	0	0	0

Johnson counters are a variation of standard ~~ring~~ ring counters, with the Inverted output of the last stage fed back to the input of the first stage.

An n-stage Johnson counter yields a count sequence of length 2n .

the advantages and disadvantages are the same as the ring counters.

• Bidirectional shift Registers:

	FF0	FF1	FF2	FF3
Clear	0	0	0	0

– each right shift operation has the effect of dividing the binary number by two, if the operation is reversed (left shift), this has the effect of multiplying the number by two.

Bidirectional shift registers can perform both operations.

3. Applications:

① To produce time delay, The amount of delay can be controlled by: 1- the number of stages in the register
2- the clock frequency.

② Convert serial data to parrallel data:

a Serial-to-parallel conversion is required in a computer or microprocessor-based systems.

The End - - - -