Philadelphia University Faculty of Engineering Department of Computer Engineering		Date:- 03/02/2014 Allowed time:- 2 Hours
Advanced Computer Architecture Final Exam		
Student Name: -…….....		ID: - ……..

Question 1:- Mark the following statements as TRUE or FALSE. 10 points

1. Resource conflict is an example of structural hazard……
2. In dynamic scheduling instruction can be executed out of order……..
3. ROB allow instructions to commit out of order……
4. In speculation Exceptions are not handled until the instruction causing it commits……..
5. Temporal locality is the locality in space……
6. Larger data Block size will decrease the miss penalty in cache miss……..
7. Pipelined cache access will decrease cache bandwidth……..
8. Merging write buffer will reduce processor stall…….
9. Simultaneous Multithreading do not allow out of order completion…….
10. symmetric multiprocessors have a centralized memory architecture……

Question 2:- List and explain the operations of the 5 stages in classic MIPS pipelined architecture. 5 points

Question 3:- Assume you have a system where 80% of the code can be parallelized, calculate the overall speed up if you use a 4 processors system comparing to 1 processor system. 4 points

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Question 4:- Assume a program that can be run in 20 seconds, and the program contains 70% integers operations , if a new system that enhance the integer operation by factor of 10 (10X speedup) is implemented what will be the new execution time of our program. 3 points

Question 5:- Assume a system that have 2 cycles hit time in L1 cache and 20 cycles hit time in L2 cache and a miss penalty 200 cycles, and the miss rate of L1 cache is 4% and the global miss rate for L2 cache is 2% calculate the average memory access time. **4 points**

Question 6:- Explain the concept of locality in cache. **2 points**

Question 7:-State the deference between Fine-Grained and Coarse-Grained Multithreading. **2 points**

Question 8:- How reorder buffer (ROB) enhance the dynamic scheduling process. **2 points**

Question 9:- Explain the operation of Correlated Branch Predictor. **3 points**

Question 10:- In a distributed memory multiprocessor architecture if the penalty of accessing remote memory location is 200 cycles, and the penalty for accessing local memory location is 50 cycles. the local cache hit is 2 cycles. If the running program have 70% instructions and the remaining are memory references(load and store instruction) and the cache miss rate is 5%, and the remote memory references are 20% of all memory references calculate the AMAT for the system above. 5 points