Philadelphia University Faculty of Engineering Department of Computer Engineering		Date:- 03/02/2014 Allowed time:- 2 Hours
Advanced Computer Architecture Final Exam		
Student Name: -…….....		ID: - ……..

Question 1:- Mark the following statements as TRUE or FALSE. **10 points**

1. Resource conflict is an example of structural hazard……TRUE…
2. In dynamic scheduling instruction can be executed out of order…TRUE…..
3. ROB allow instructions to commit out of order…FALSE…
4. In speculation Exceptions are not handled until the instruction causing it commits…TRUE…
5. Temporal locality is the locality in space…FALSE……
6. Larger data Block size will decrease the miss penalty in cache miss…FALSE…..
7. Pipelined cache access will decrease cache bandwidth…FALSE…..
8. Merging write buffer will reduce processor stall…TRUE….
9. Simultaneous Multithreading do not allow out of order completion…FALSE….
10. symmetric multiprocessors have a centralized memory architecture…TRUE…

Question 2:- List and explain the operations of the 5 stages in classic MIPS pipelined architecture. 5 points

1. **Instruction fetch The next instruction is fetched from the memory address that is currently stored in the program counter (PC), and stored in the instruction register (IR)**
2. **Instruction Decode: The decoder interprets the instruction. During this cycle the operand is red in to registers**
3. **Execute: in this stage the instruction is executed using ALU .**
4. **Memory access: load and store operations is performed in this stage**
5. **Write back: write the result of instruction in to destination register**

Question 3:- Assume you have a system where 80% of the code can be parallelized, calculate the overall speed up if you use a 4 processors system comparing to 1 processor system. **4 points**

$$speedup_{overall} = \frac{1}{(1 - fraction_{parallel}) + \frac{fraction_{parallel}}{speedup_{parallel}}}$$

$$speedup_{overall} = \frac{1}{(1 - 0.8) + \frac{0.8}{4}}$$

$$speedup_{overall} = \frac{1}{0.2 + 0.2}$$

$$speedup_{overall} = \frac{1}{0.4} = 2.5$$

Question 4:- Assume a program that can be run in 20 seconds, and the program contains 70% integers operations , if a new system that enhance the integer operation by factor of 10 (10X speedup) is implemented what will be the new execution time of our program. **3 points**

$$ExecTime_{new} = ExecTime_{old} \times (1 - fraction_{enhanced} + \frac{fraction_{enhanced}}{speedup_{enhanced}})$$

$$ExecTime_{new} = 20 \times (1 - 0.7 + \frac{0.7}{10})$$

$$ExecTime_{new} = 20 \times (0.3 + 0.07) = 20 \times 0.37 = 7.4\ seconds$$

Question 5:- Assume a system that have 2 cycles hit time in L1 cache and 20 cycles hit time in L2 cache and a miss penalty 200 cycles, and the miss rate of L1 cache is 4% and the global miss rate for L2 cache is 2% calculate the average memory access time. **4 points**

$$AMAT = HitTime_{L1} + miss\ rate_{L1} \times Hit\ Time_{L2} + global\ miss\ rate_{L2} \times miss\ penalty$$

$$AMAT = 2 + 0.04 \times 20 + 0.02 \times 200$$

$$AMAT = 2 + 0.08 + 4 = 6.8\ cycles$$

Question 6:- Explain the concept of locality in cache. **2 points**

1. **Temporal Locality (Locality in Time): If an item is referenced, it will tend to be referenced again soon (e.g., loops, reuse)**
2. **Spatial Locality (Locality in Space): If an item is referenced, items whose addresses are close by tend to be referenced soon**

Question 7:-State the deference between Fine-Grained and Coarse-Grained Multithreading. **2 points**

1. **Fine-Grained Switches between threads on each instruction, causing the execution of multiples threads to be interleaved, skipping any stalled threads, CPU must be able to switch threads every clock**
2. **Coarse-Grained Switches threads only on costly stalls, such as L2 cache misses**

Question 8:- How reorder buffer (ROB) enhance the dynamic scheduling process. **2 points**

Overcome control dependence by hardware speculating on outcome of branches and executing program as if guesses were correct

separate execution from allowing instruction to finish or "commit" where instructions commit only if the result of branch prediction is correct and can undo the result of speculation if the result of branch prediction is incorrect

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Question 9:- Explain the operation of Correlated Branch Predictor. **3 points**

Correlated branch predictor use the lower n bits of branch address to select from 2^n entry of local branch history table and it uses the last m global branches to select a local table from 2^m local branch history table

(m,n) branch predictor

Question 10:- In a distributed memory multiprocessor architecture if the penalty of accessing remote memory location is 200 cycles, and the penalty for accessing local memory location is 50 cycles. the local cache hit is 2 cycles. If the running program have 70% instructions and the remaining are memory references(load and store instruction) and the cache miss rate is 5%, and the remote memory references are 20% of all memory references calculate the AMAT for the system above. 5 points

$$AMAT_{INSTRUCTIONS} = HitTime + miss\ rate\ \times miss\ penalty_{INSTRUCTIONS}$$

$$AMAT_{INSTRUCTIONS} = 2 + 0.05\ \times 50 = 2 + 2.5 = 4.5\ cycles$$

$$AMAT_{DATA} = HitTime + miss\ rate\ \times miss\ penalty_{DATA}$$

$$miss\ penalty_{DATA} = fraction_{local}\ miss\ penalty_{local} + fraction_{remotr} miss\ penalty_{remote}$$

$$miss\ penalty_{DATA} = 0.8\ \times 50 + 0.2\ \times 200 = 40 + 40 = 80\ cycles$$

$$AMAT_{DATA} = 2 + 0.05\ \times 80 = 6\ cycles$$

$$AMAT = fraction_{instruction} \times AMAT_{instructions} + fraction_{data} \times AMAT_{data}$$

$$AMAT = 0.7 \times 4.5 + 0.2 \times 6$$

$$AMAT = 3.15 + 1.8 = 4.95\ cycles$$